

LCFC Confidential


G Project M/B Schematics Document

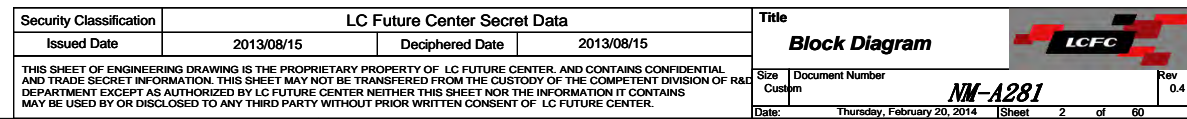
AMD FT3B Beema SOC with DDRIIL

AMD JET-LE

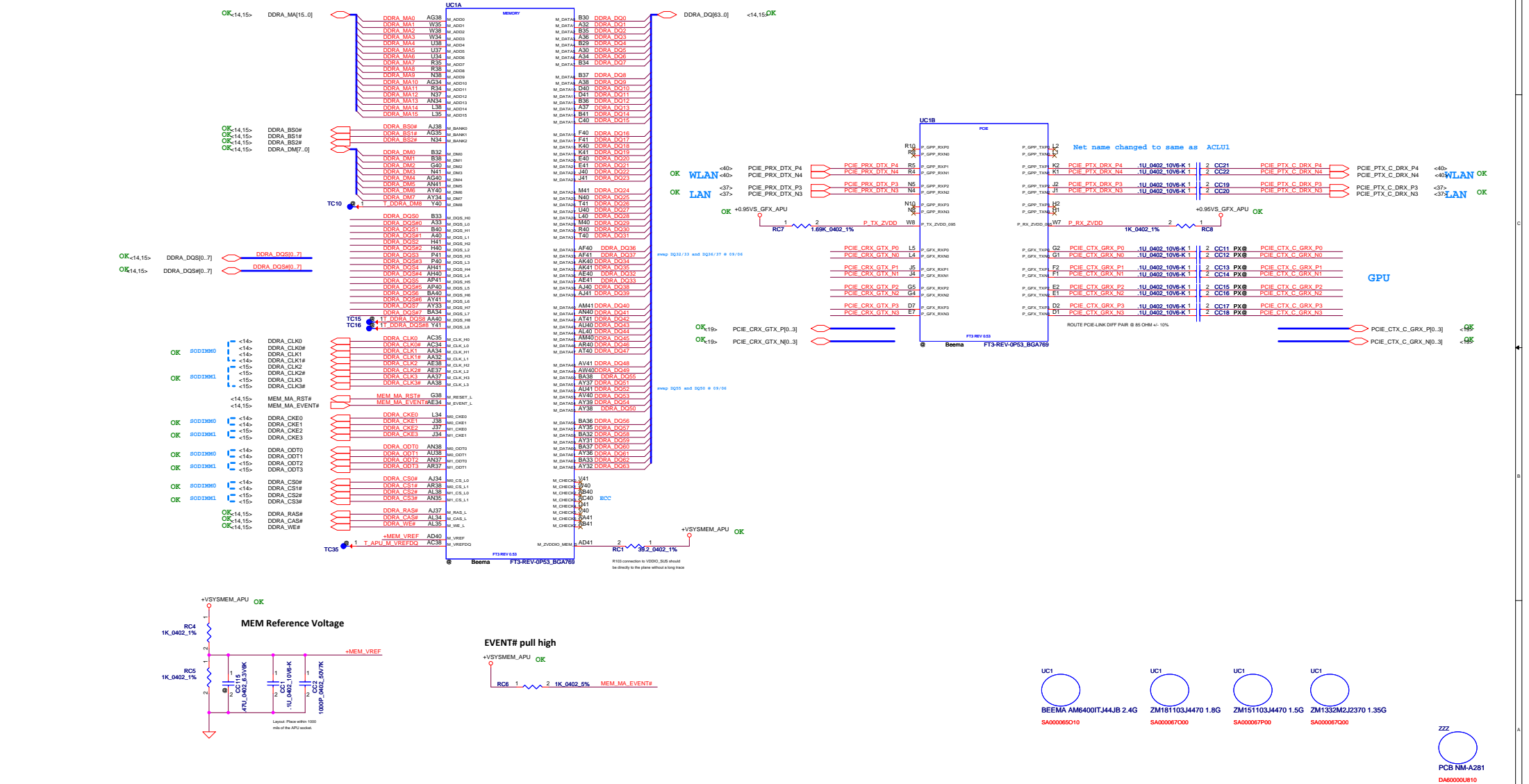
2014-2-12

REV:0.4

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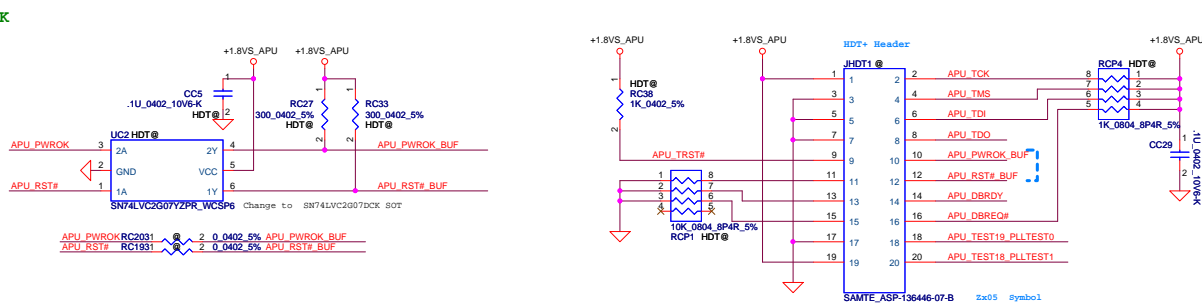
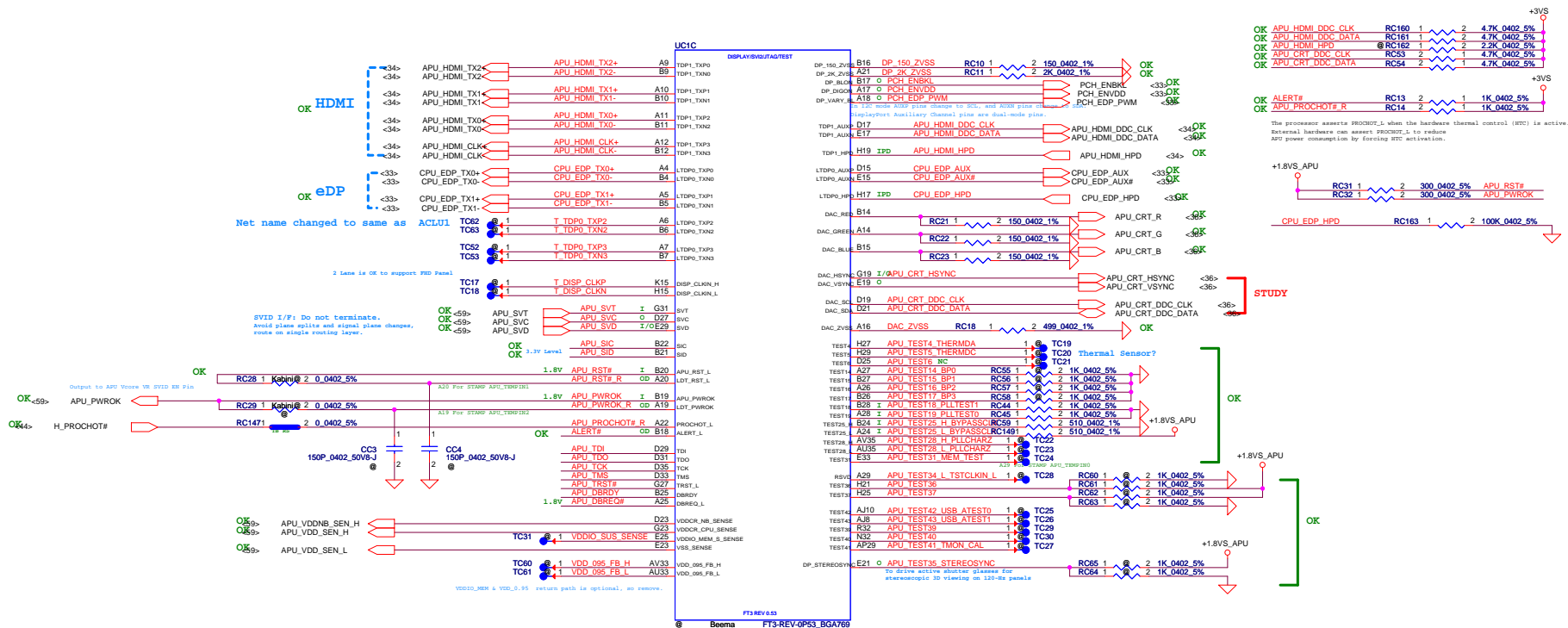
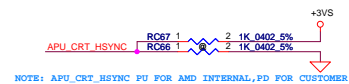
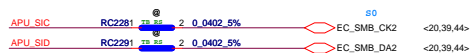


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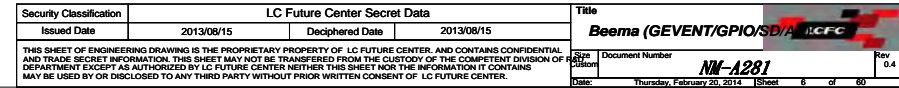
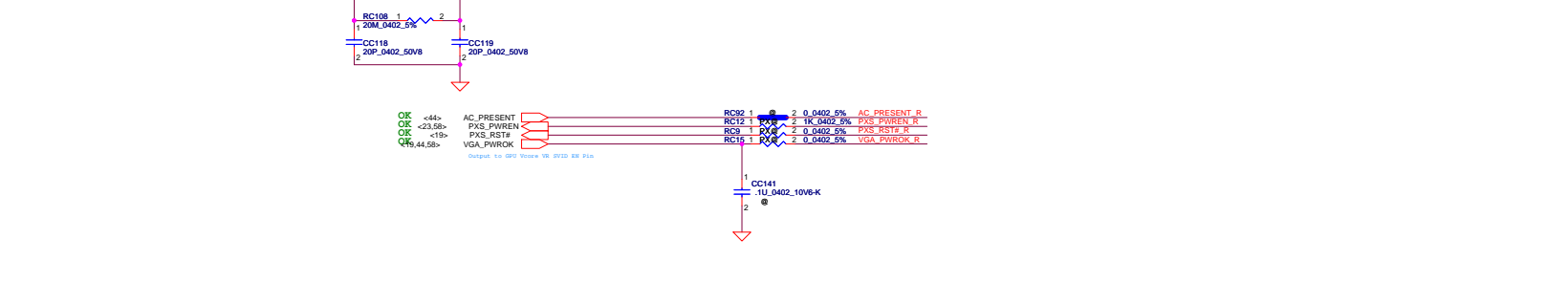
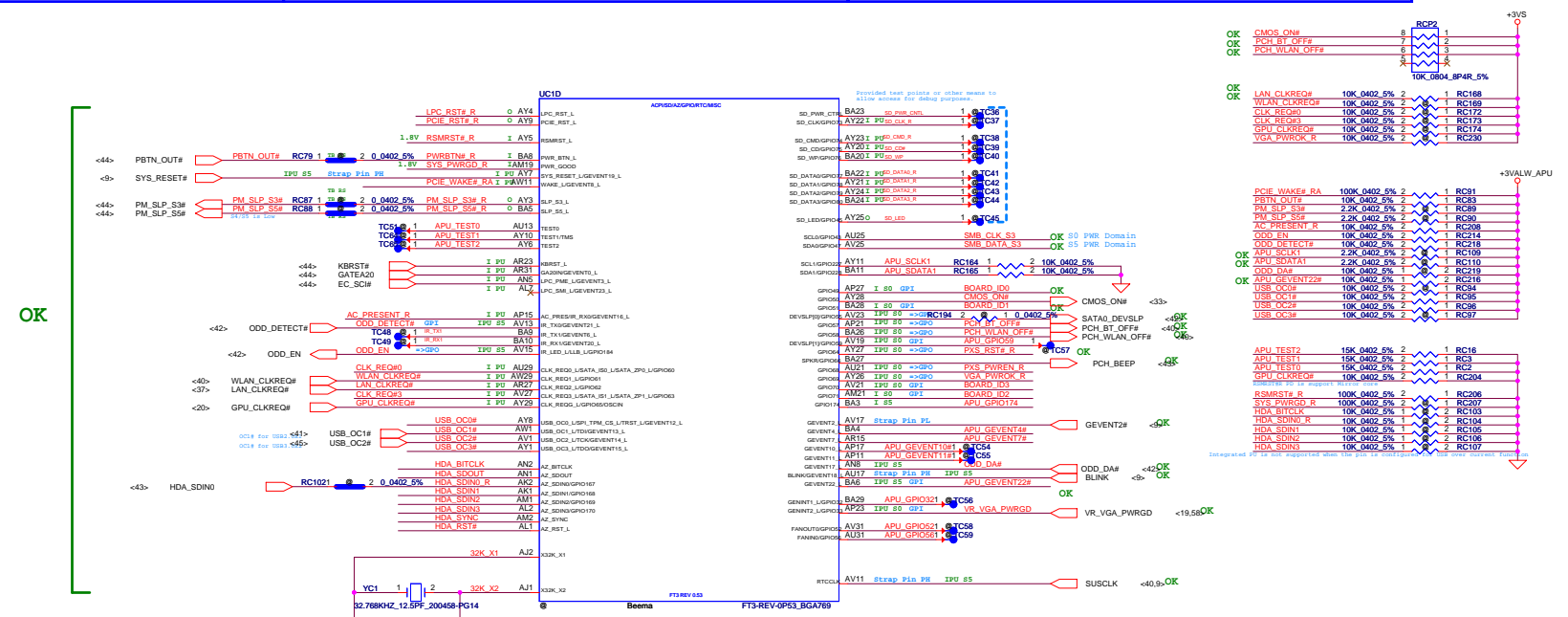
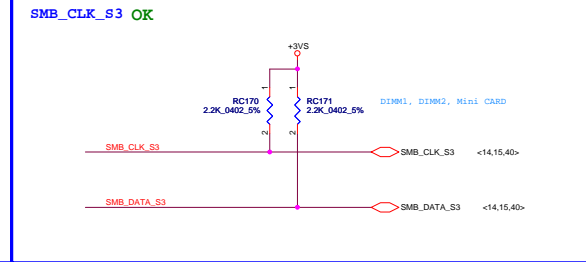


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Beema (DISPLAY/CLK/MISC)



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48MHz/10pF Crystal

48M_X1

48M_X2 OK

RC191 1 2 1M_0402_5%

YC2

OSC1 NC1 NC2 OSC2

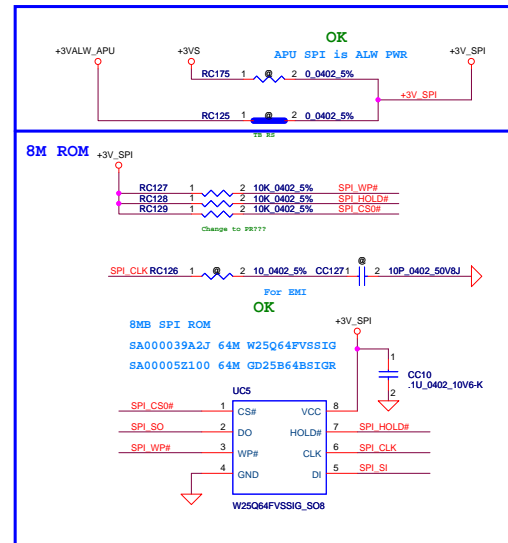
48MHZ_10PF_7V480000017

CC123 1 2 12P_0402_50V8-J

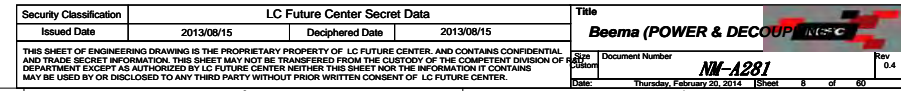
CC124 1 2 12P_0402_50V8-J

SJ10000IO00 TXC: 7V48000017 (48MHz)

Change to 15pF as vendor suggest



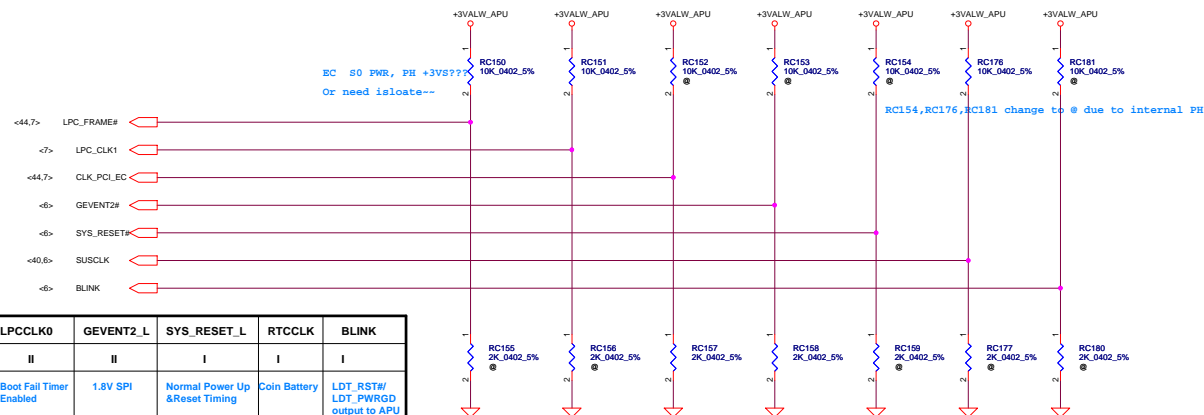
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		NM-A281		0.4	
Date:		Thursday, February 20, 2014		Sheet 7 of 60	




STRAP PINS


Signal	LFRAME_L	LPCCLK1	LPCCLK0	GEVENT2_L	SYS_RESET_L	RTCCLK	BLINK
Type	II	II	II	II	I	I	I
PULL HIGH	SPI ROM Default	Internal CLK Gen Default	Boot Fail Timer Enabled	1.8V SPI	Normal Power Up & Reset Timing Default	Coin Battery Default	LDT_RST#/ LDT_PWRGD output to APU Default
PULL LOW	LPC ROM	External CLK Gen	Boot Fail Timer Disabled Default	3.3V SPI Default	Reserved	Direct DC	Reserved


Type I straps become valid immediately after capture with the rising edge of RSMRST_L.
Type II straps become valid after PWR_GOOD is asserted
All Strap pins must be configured with either external pull-up or pull-down resistors.

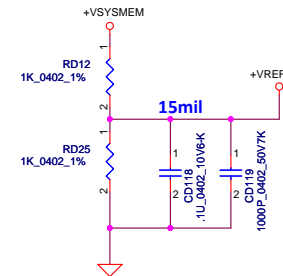
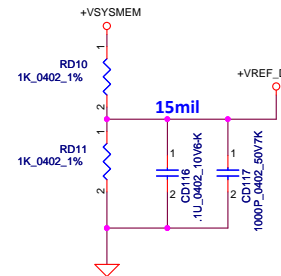
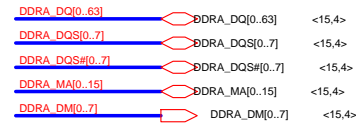
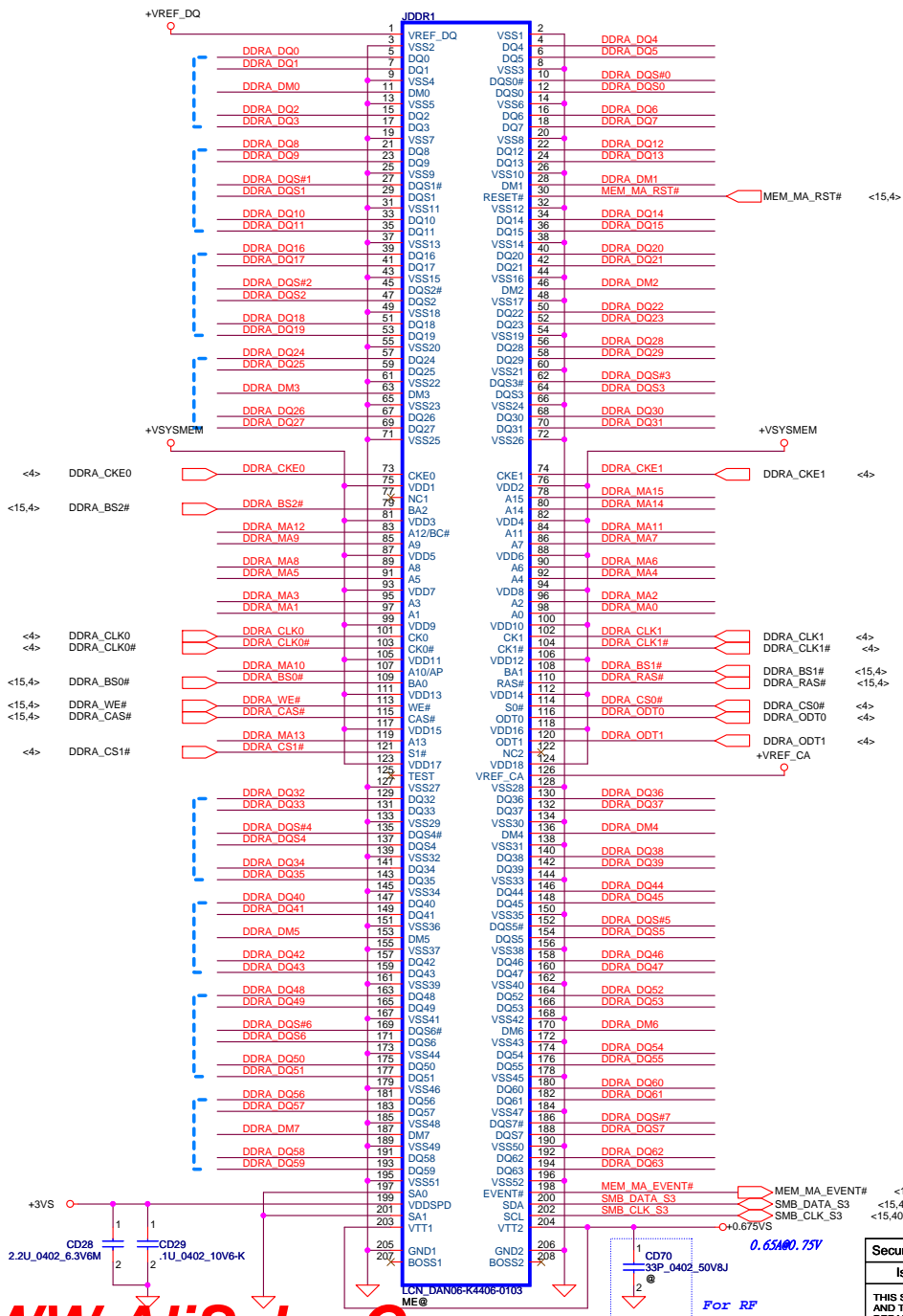


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				Date:	Thursday, February 20, 2014	Sheet 10 of 80

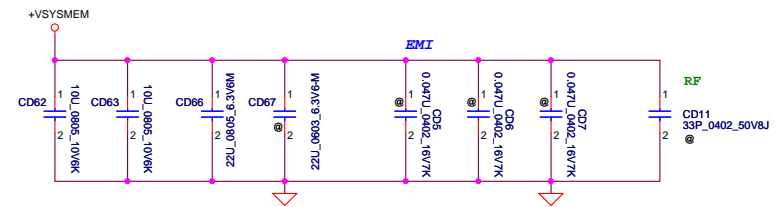
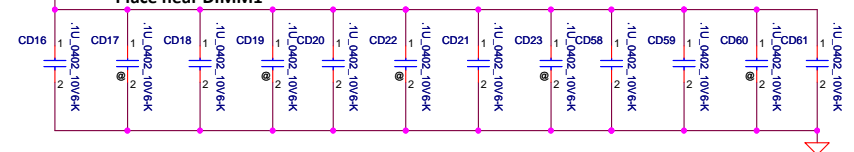
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				Date:	Thursday, February 20, 2014	Sheet
						12 of 80

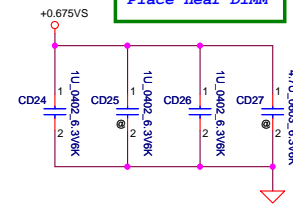
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				Date: Thursday, February 20, 2014	Sheet 13 of 60

DDR3 SO-DIMM A


Layout Note:
Place near DIMM1



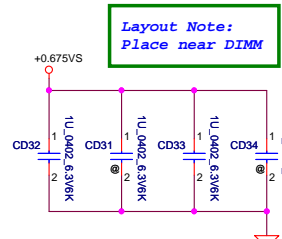
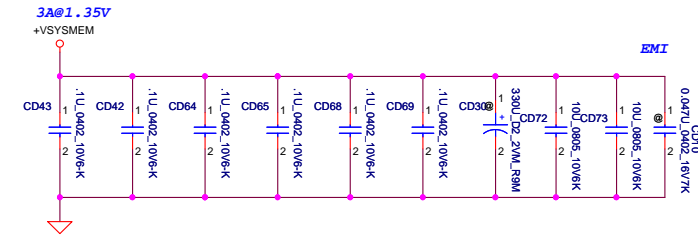
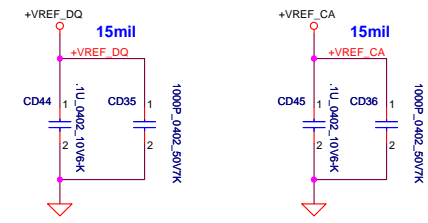
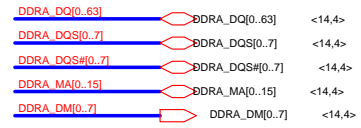
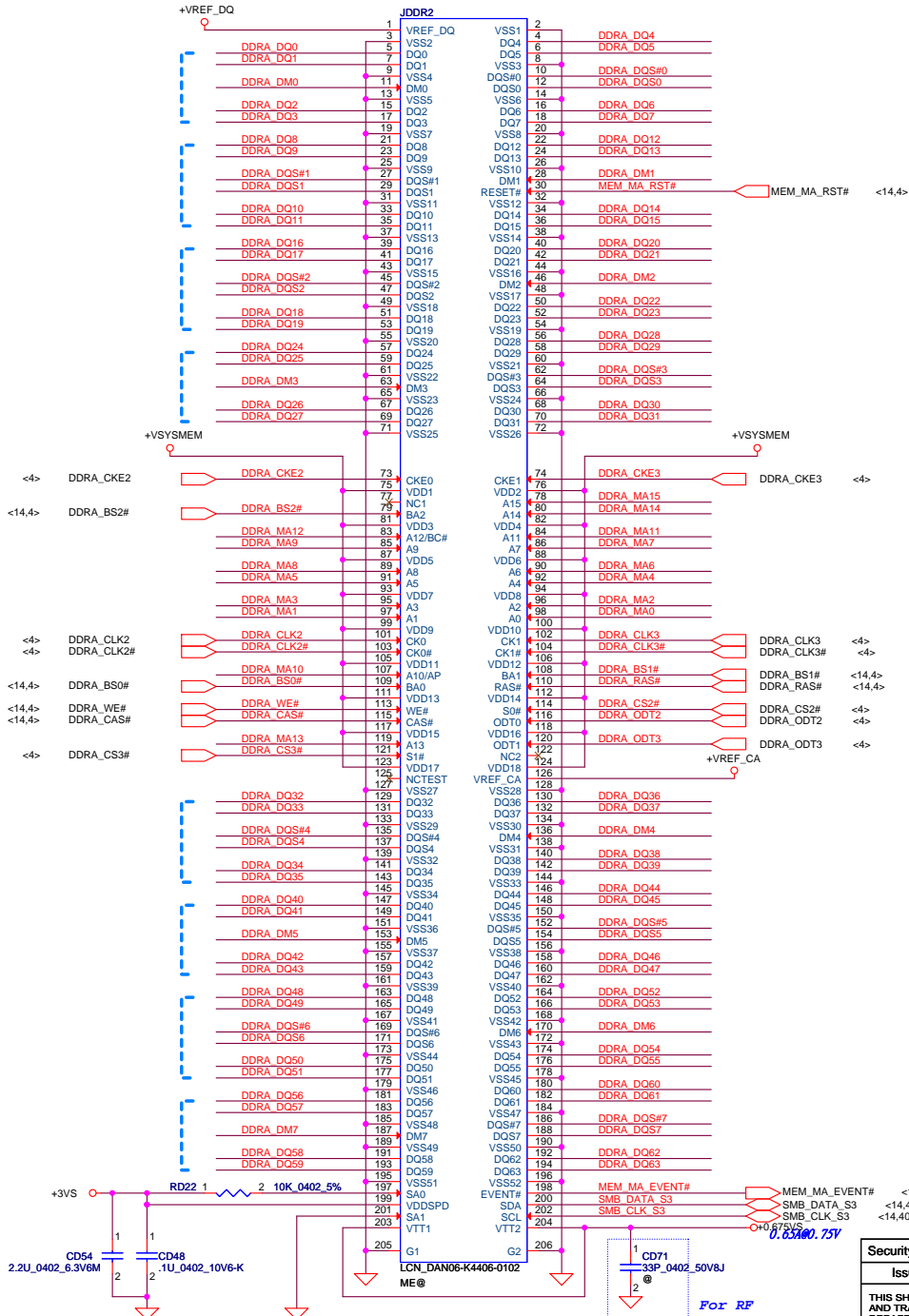
Layout Note:
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DDR3 SO-DIMM B



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Size		Document Number		Rev					
Custom		NM-A281		0.4					
Date:		Thursday, February 20, 2014				Sheet		15 of 60	

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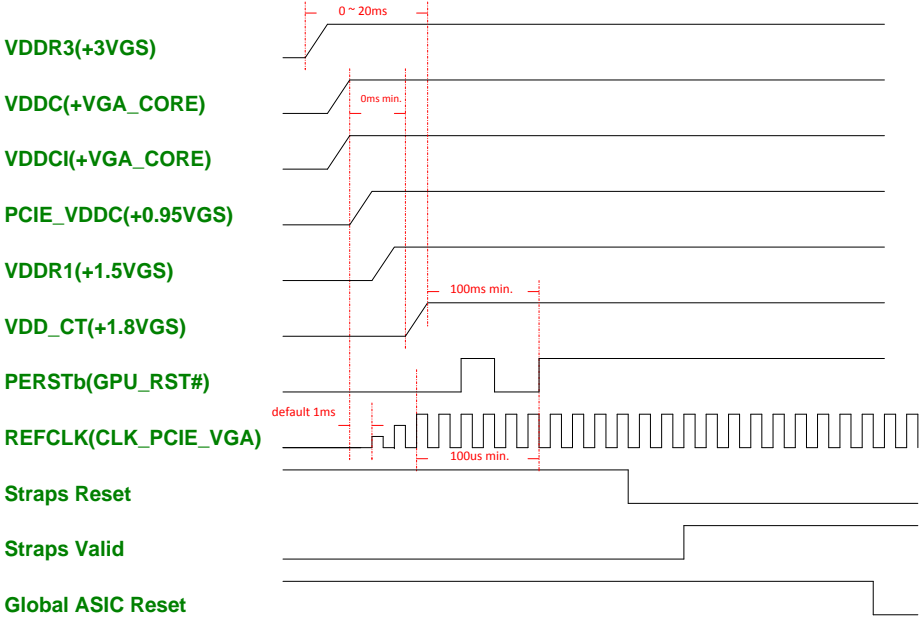
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		Size	Document Number	Rev
		Custom	NM-A281	0.4
		Date:		Thursday, February 20, 2014
		Sheet		17 of 60

VGA Note list need to be update!

Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

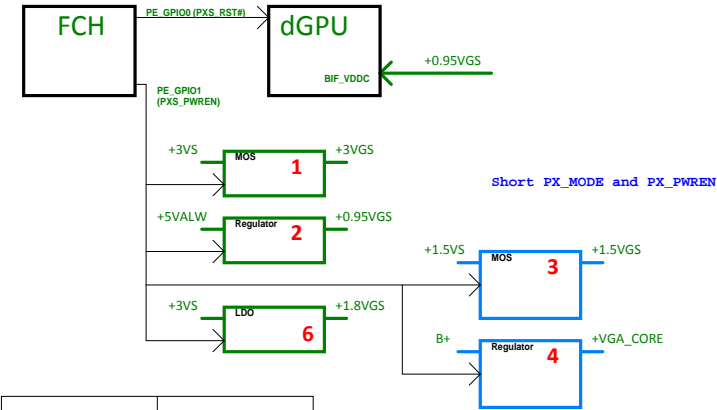


Without BACO option :

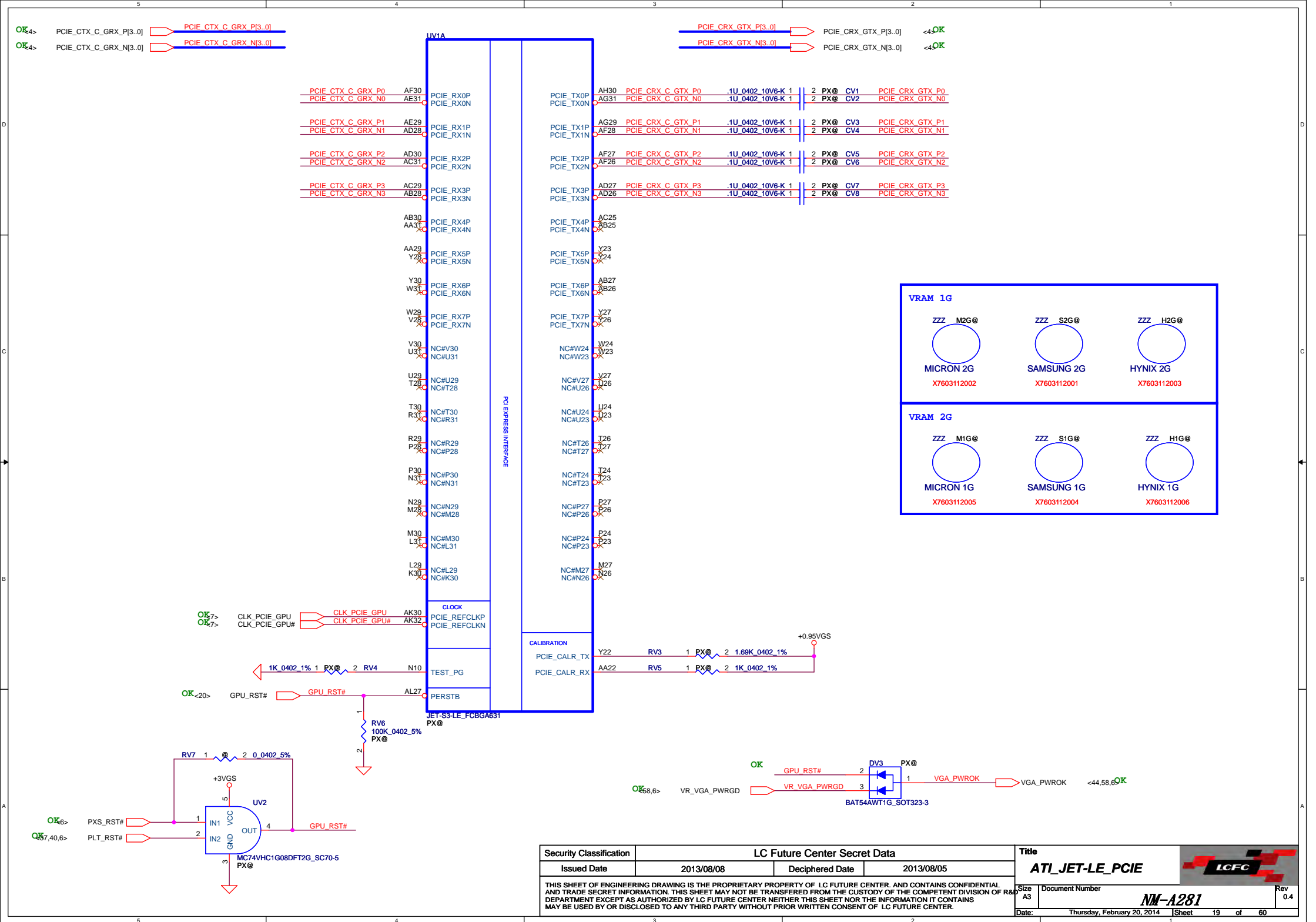
PE_GPIO0 : Low -> Reset dGPU ; High -> Normal operation
PE_GPIO1 : Low -> dGPU Power Off ; High -> dGPU Power ON

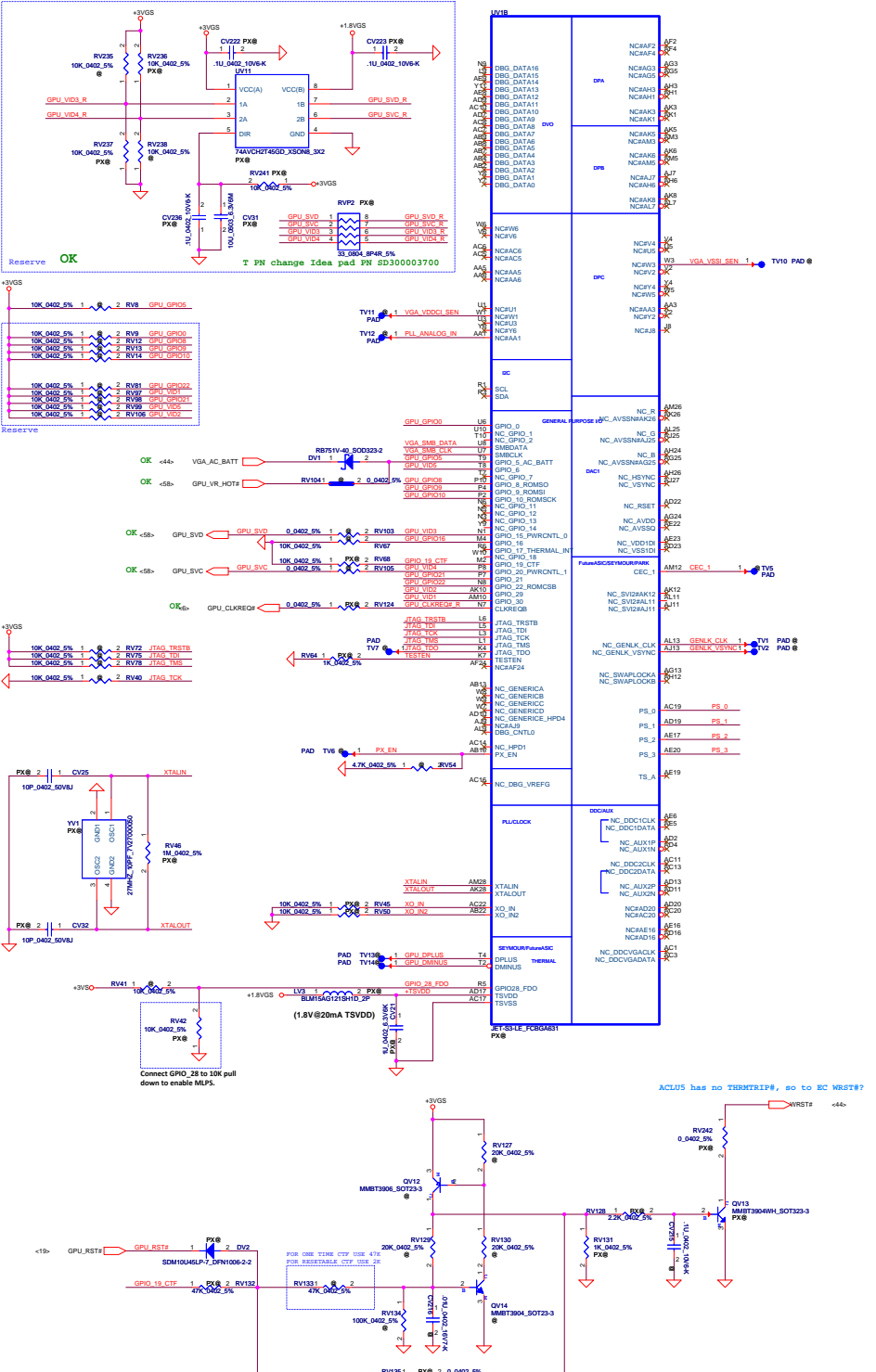
dGPU Power Pins	Voltage	Max current
VDD_CT, DP_VDDR, SPLL_PVDD, MPLL_PVDD, PCIE_PVDD, TSVDD, VDDR4, AVDD, VDD1DI	1.8V	1243mA
DP_VDDC, SPLL_VDDC, PCIE_VDDC, BIF_VDDC	0.95V	4560mA
VDDR3	3.3V	25mA
VDDR1	1.5V	1.5A
VDDC	0.8~1.125V	TBD
VDDCI	0.8~1.1V	8.8A

PX5.5



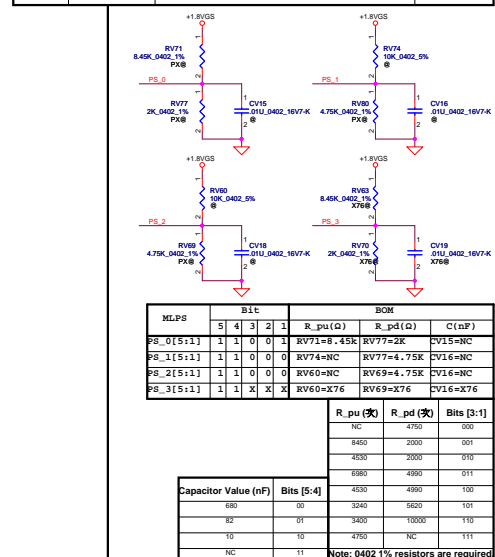
Name	Pin Assignment
PE_GPIO0	GPIO191
PE_GPIO1	GPIO192





CONFIGURATION STRAPS

ALLOW FOR PULL UP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				RECOMMENDED SETTINGS
MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS	
PS_[0]	ROM_CONFIG[0]	Define the ROM type when STRAP_BIOS_ROM_EN = 1	0 = DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE	
PS_[1]	ROM_CONFIG[1]	Define the primary memory aperture size when STRAP_BIOS_ROM_EN = 0	100 = 256MB	X
PS_[4]	NA	Reserved for internal use only. Must be 1 at reset.		1
PS_[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.		X
PS_[11]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	0 = Not support	X
PS_[12]	STRAP_BIF_CLK_PA_EN	0 = The CLKREQ power management capability is disabled. 1 = The CLKREQ power management capability is enabled.		0
PS_[13]	NA	Reserved for internal use only. Must be 0 at reset.		0
PS_[14]	STRAP_TX_CPO_DRV_LULL_SWING	0 = The transmitter full-swing is enabled. 1 = The transmitter full-swing is disabled.		1
PS_[15]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	1 = Enable	X
PS_[21]	NA	Reserved.		NA
PS_[22]	NA	Reserved.		NA
PS_[23]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0 = Disable	X
PS_[24]	STRAP_BIF_VGA_DIS_SELECTOR	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.		0
PS_[25]	NA	Reserved.		NA
PS_[31]	BOARD_CONFIG[0]	Board configuration related straps, such as for memory ID	100 = Hynix IG 110 = Micron IG 111 = Samsung IG	X
PS_[32]	BOARD_CONFIG[1]	Board configuration related straps, such as for memory ID	100 = Hynix IG 110 = Micron IG 111 = Samsung IG	X
PS_[33]	BOARD_CONFIG[2]	Board configuration related straps, such as for memory ID	100 = Hynix IG 110 = Micron IG 111 = Samsung IG	X
PS_[34]	AUD_PORT_CONN_PINSTRAP[1]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user. (Combine with PS_[35])	111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	X
PS_[35]	AUD_PORT_CONN_PINSTRAP[2]			



UV1F

NC_VARY_BL
NC_DIGON

AB11
AB12

NC_UPHYAB_TMDPA_TX0N
NC_UPHYAB_TMDPA_TX0P
NC_UPHYAB_TMDPA_TX1N
NC_UPHYAB_TMDPA_TX1P

AL15
AK14
AH16
AJ15

NC_UPHYAB_TMDPA_TX2N
NC_UPHYAB_TMDPA_TX2P

AL17
AK16

NC_UPHYAB_TMDPA_TX3N
NC_UPHYAB_TMDPA_TX3P

AH18
AJ17

NC_TXOUT_L3P
NC_TXOUT_L3N

AL19
AK18

TMDP

NC_UPHYAB_TMDPB_TX0N
NC_UPHYAB_TMDPB_TX0P

AH20
AJ19

NC_UPHYAB_TMDPB_TX1N
NC_UPHYAB_TMDPB_TX1P

AL21
AK20

NC_UPHYAB_TMDPB_TX2N
NC_UPHYAB_TMDPB_TX2P

AH22
AJ21


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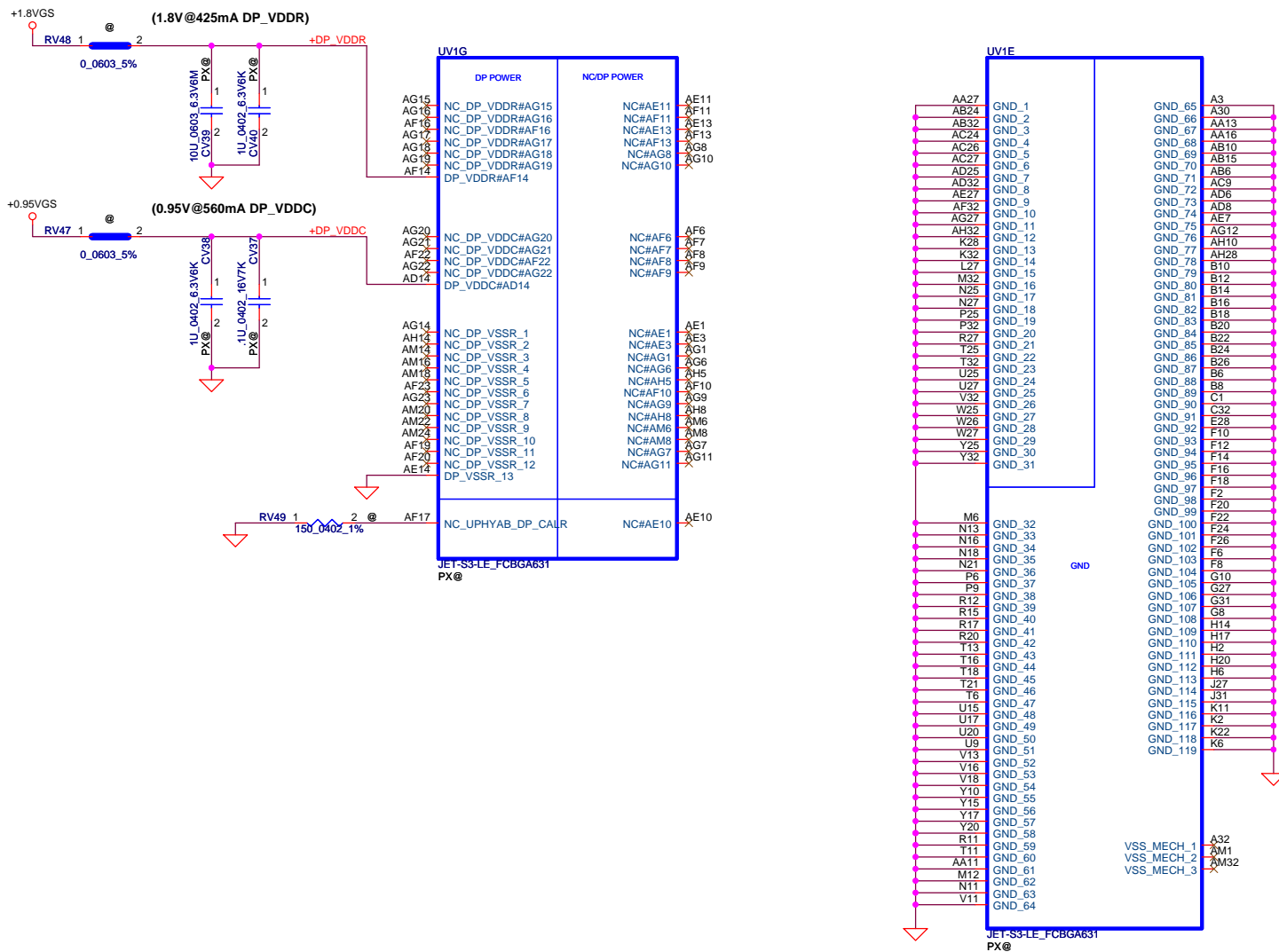
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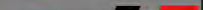
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NC_TXOUT_U3N

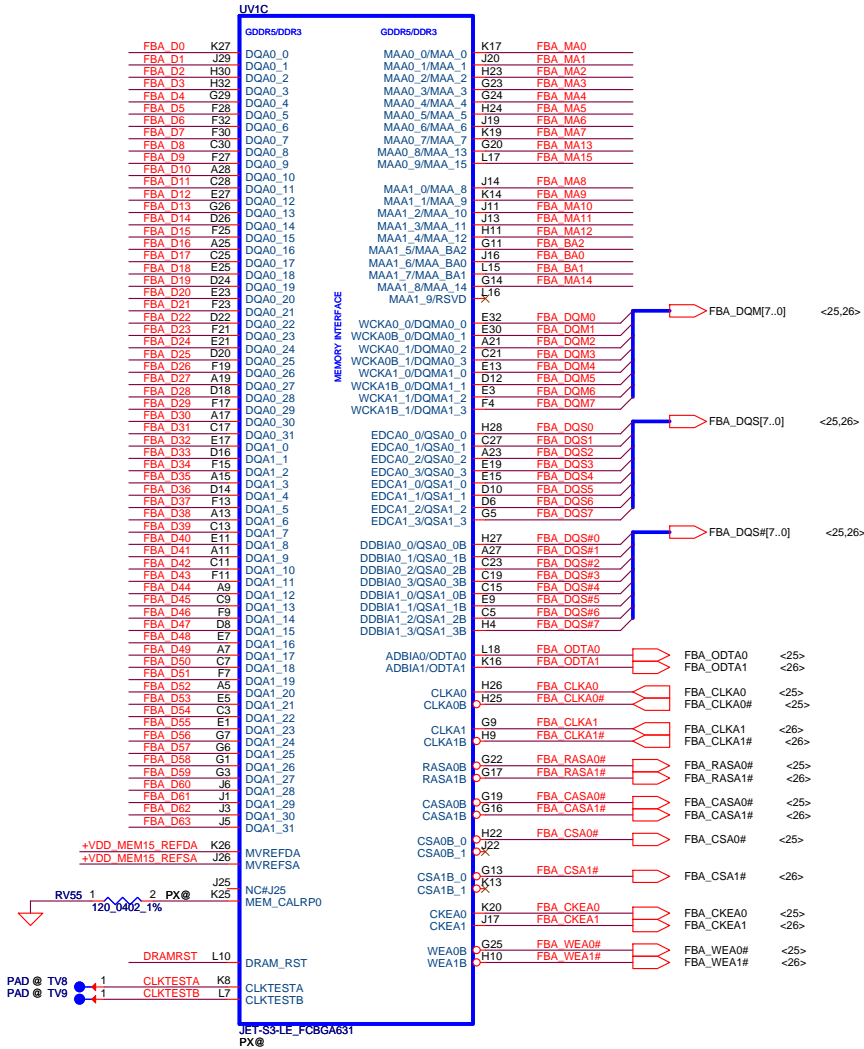
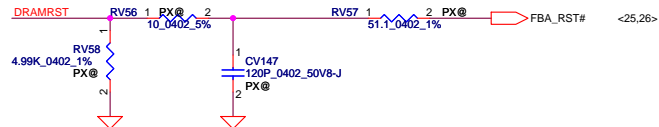
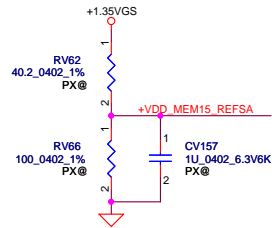
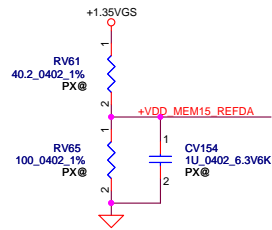
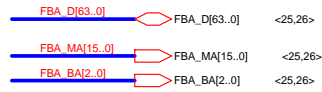
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AJ23

JET-S3-LE_FCBGA631
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						Custom	NM-A281	0.4
						Date:	Thursday, February 20, 2014	Sheet 21 of 60

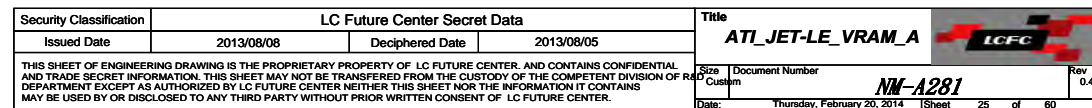


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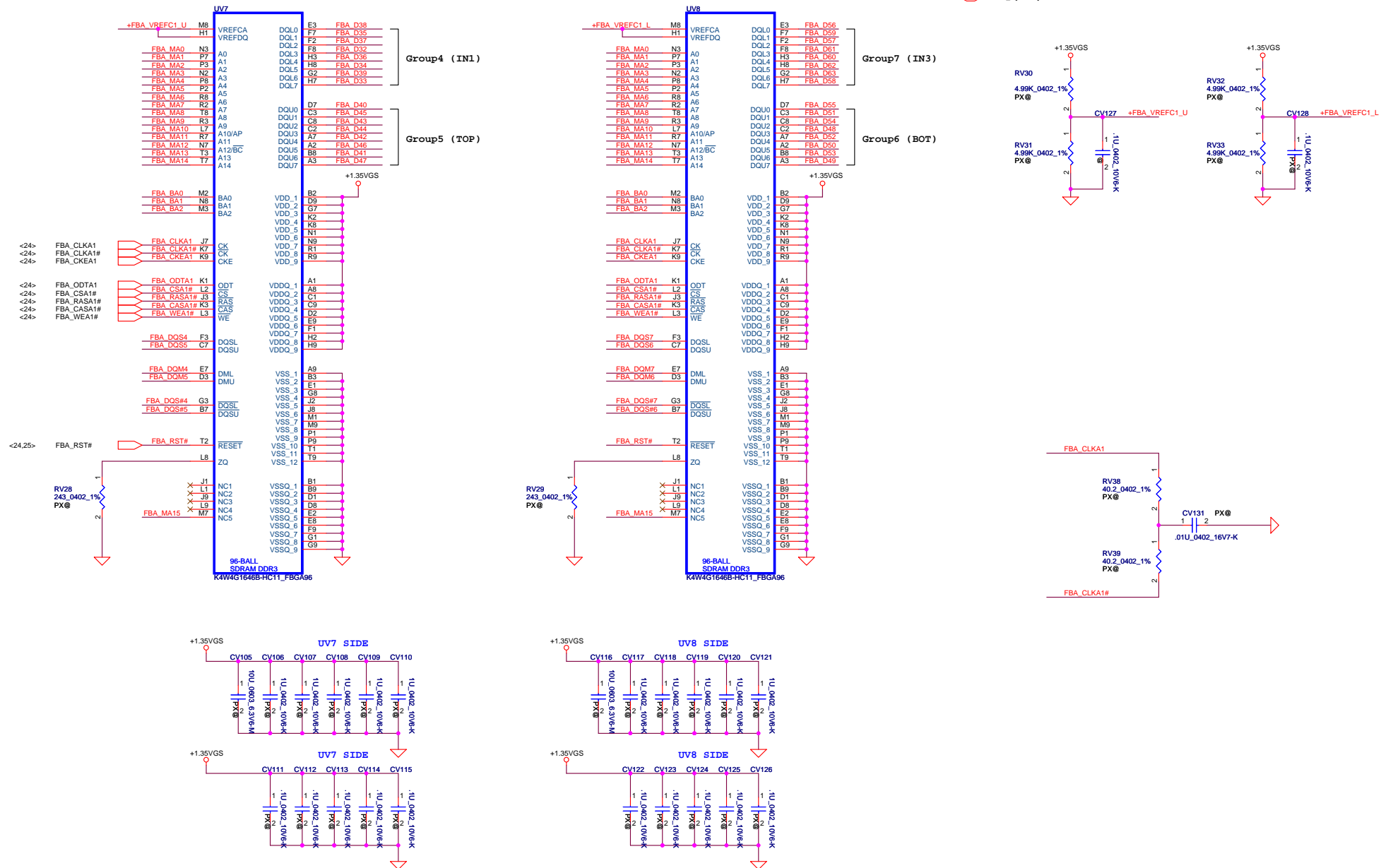



Security Classification		LC Future Center Secret Data		Title	
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				Document Number	NM-A281
				Date: Thursday, February 20, 2014	Sheet 24 of 60

FBA_MA[15..0]	<24,26>	ACL05 swap the VRAM Data @ 08/26
FBA_BA[2..0]	<24,26>	VRAM 8 pcs change to 4 pcs @ 09/26
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FBA_DQM[3..0]	<24>	
FBA_DQS[3..0]	<24>	
FBA_D[31..0]	<24>	






Memory Partition A - Upper 32 bits



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		Security Classification		LC Future Center Secret Data		Title			
		Issued Date		2013/08/08		Deciphered Date		2013/08/05	
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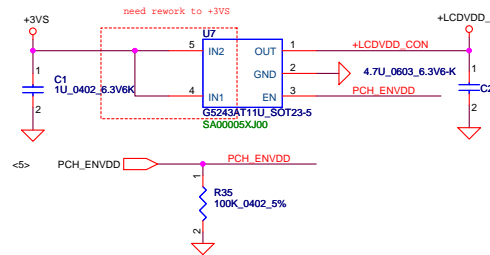
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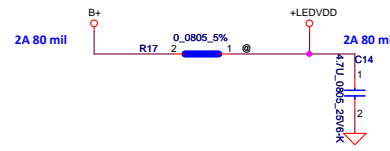
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LCD POWER CIRCUIT OK

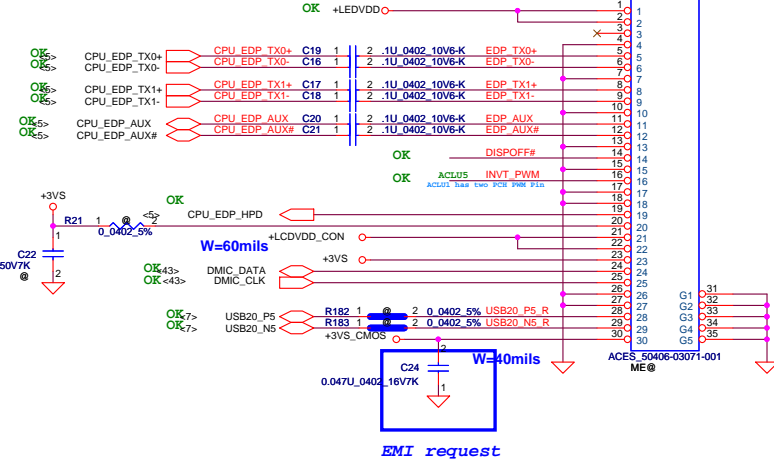
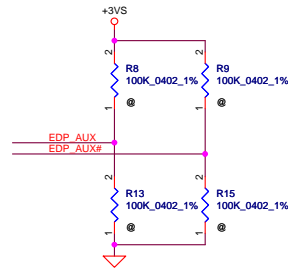
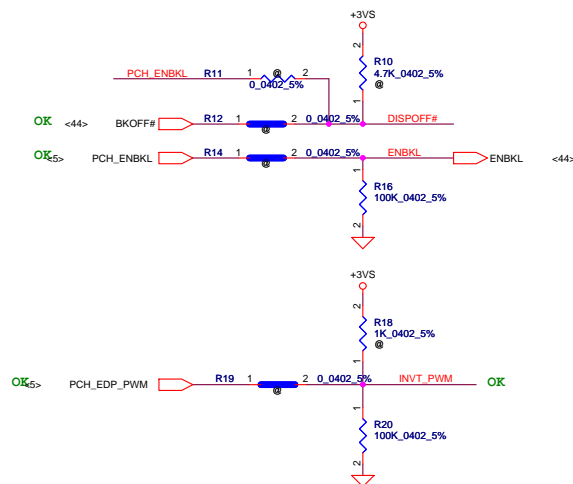
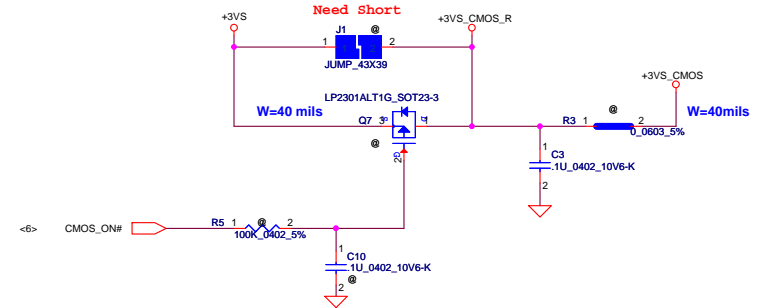


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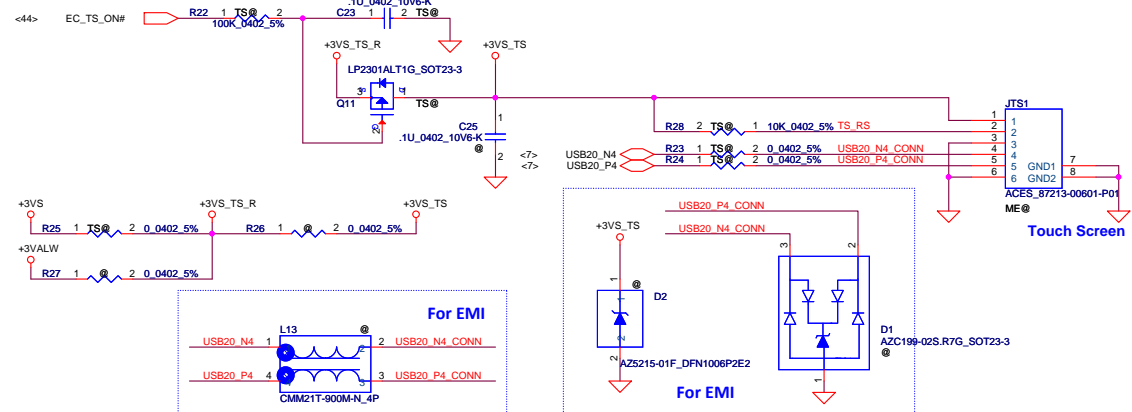


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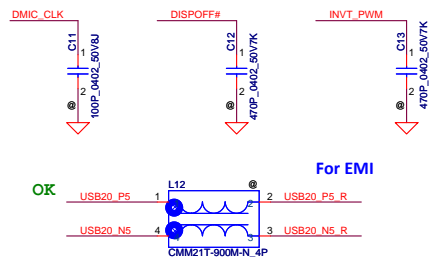
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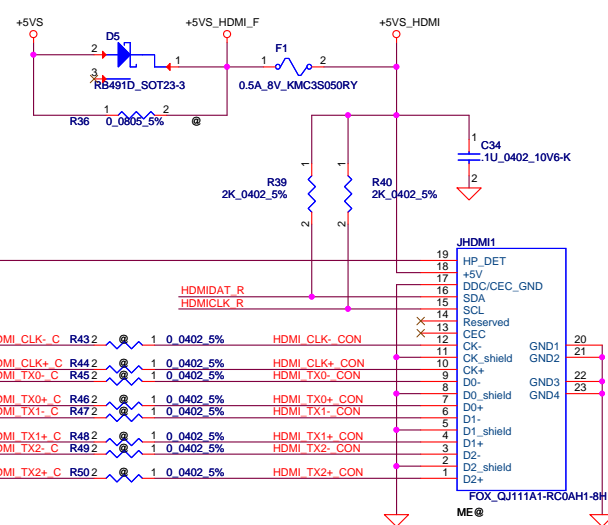
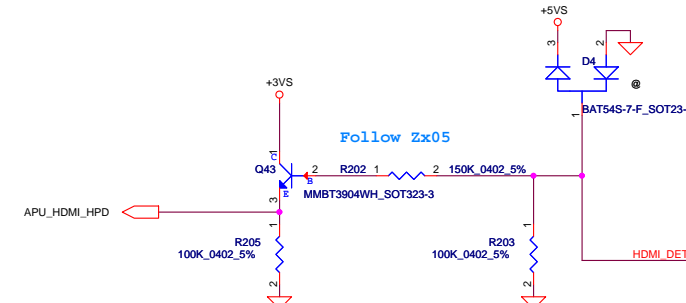
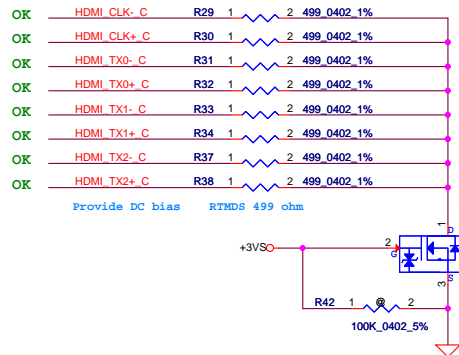
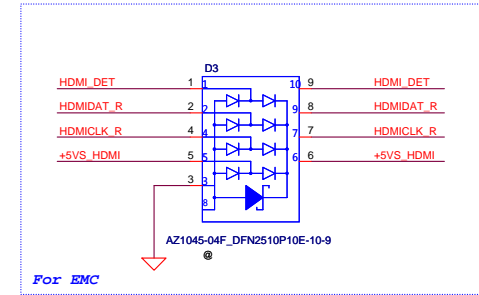
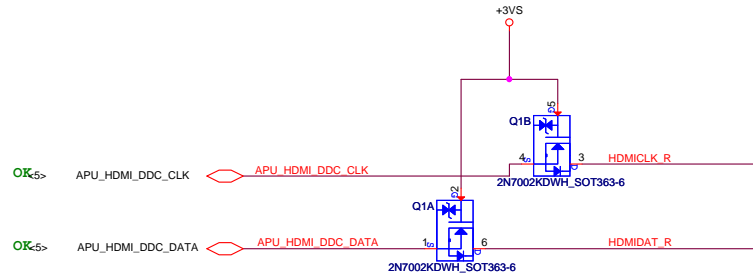
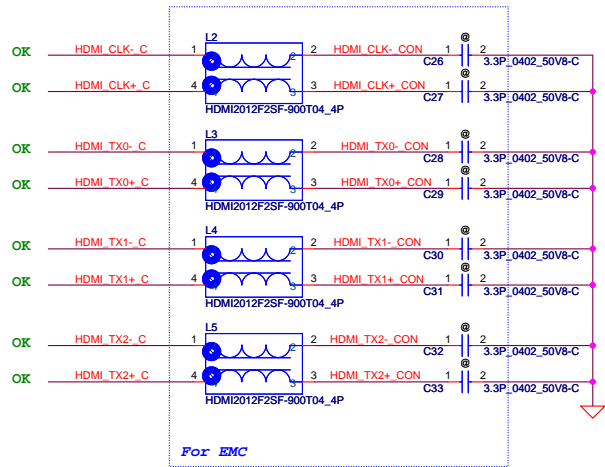
Touch Screen OK



EMI request

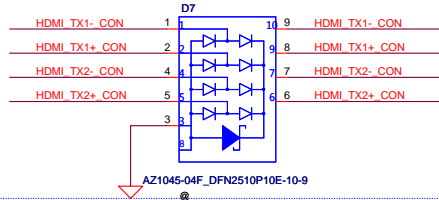
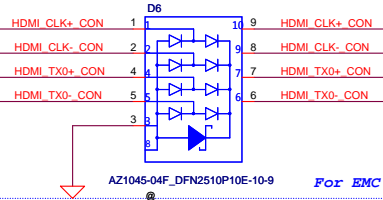



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				Size Custom	Document Number NM-A281	Rev 0
				Date:	Thursday, February 20, 2014	Sheet 33 of 60




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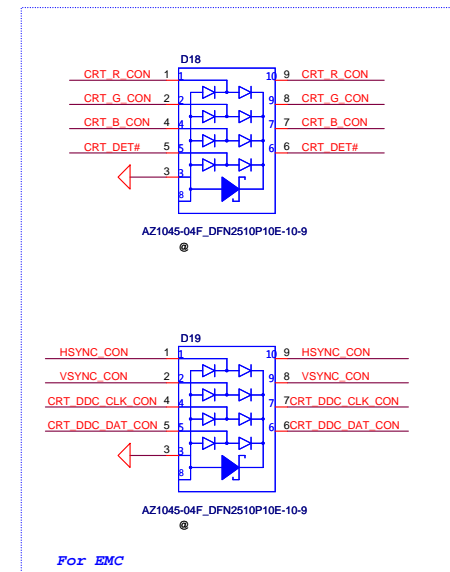
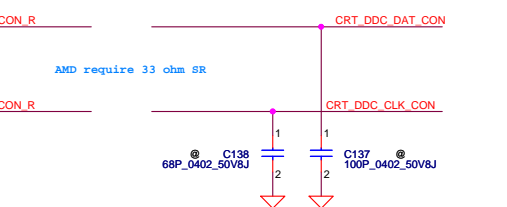
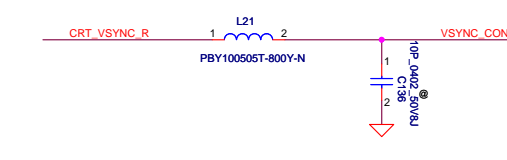
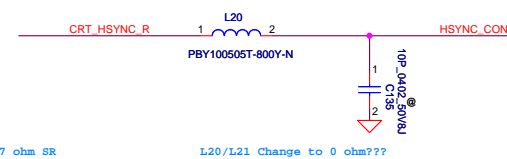
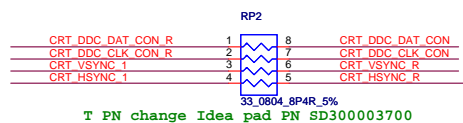
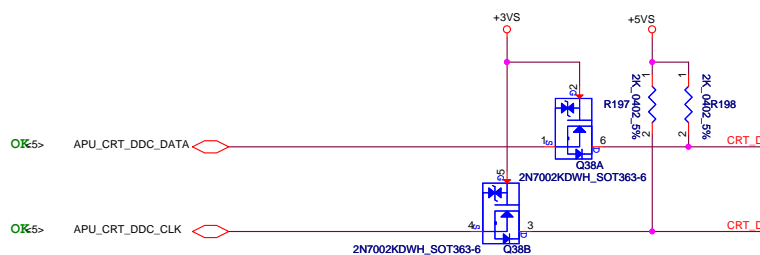
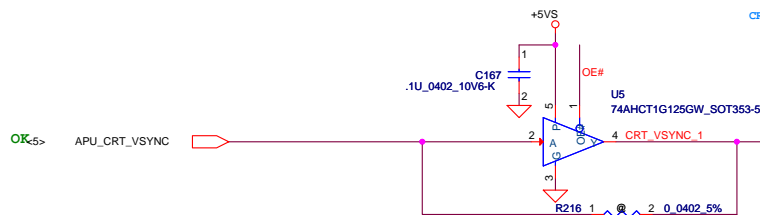
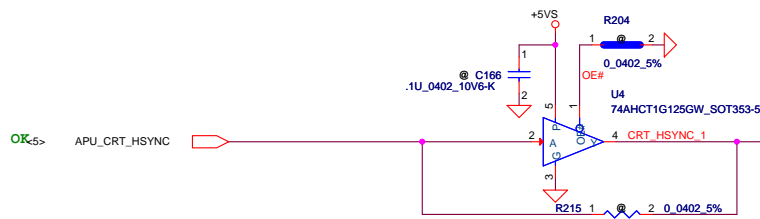
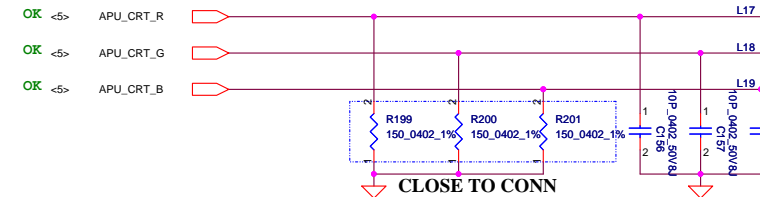
Close to JHDMI1



Security Classification		LC Future Center Secret Data				Title									
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										Date:		Thursday, February 20, 2014		Sheet 34 of 60	

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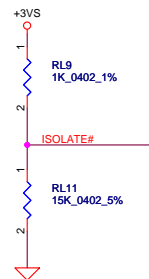
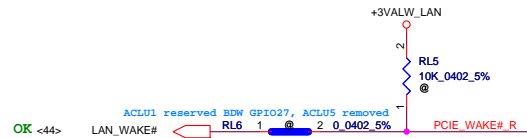
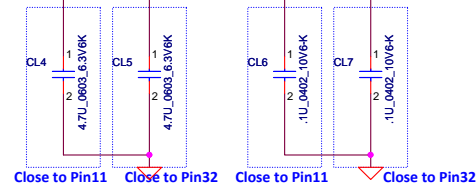
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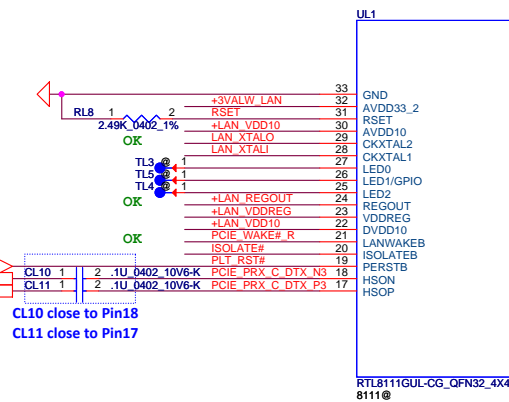
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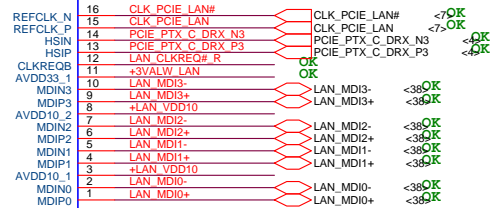
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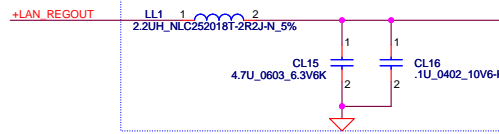
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OK <4>



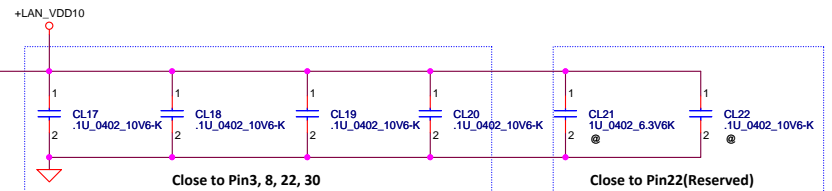
CL10 close to Pin18
CL11 close to Pin17



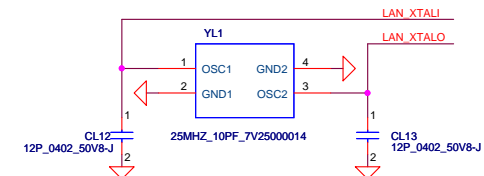
For RTL8111GUL/RTL8106EUL (SWR mode)



Layout Note: LL1 must be within 200mil to Pin36,
CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

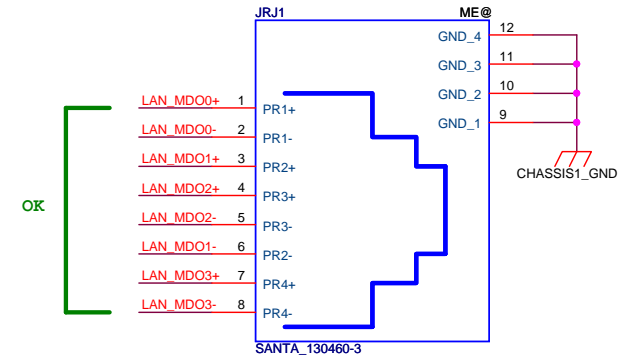
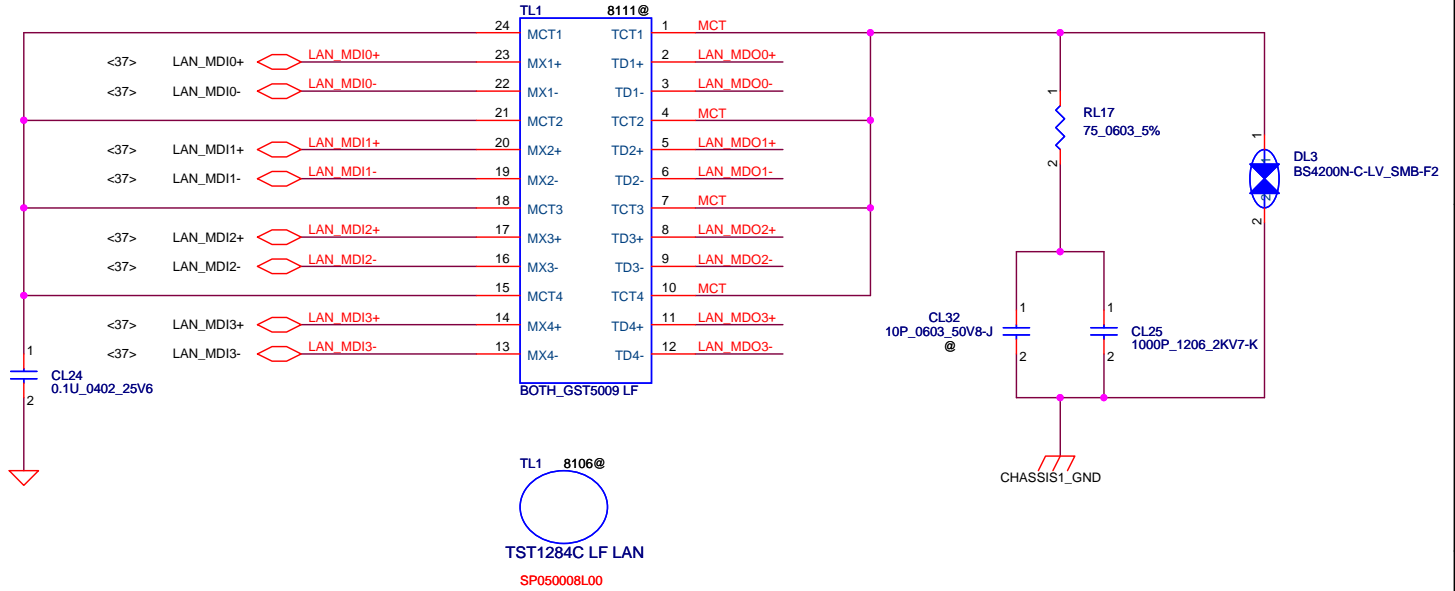
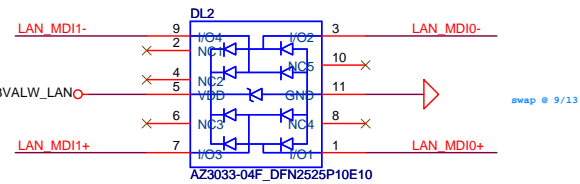
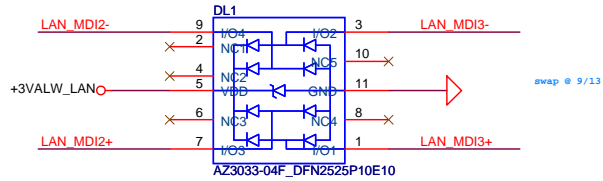


LAN ROM OK

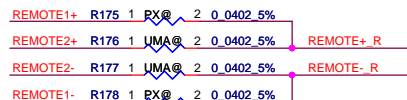
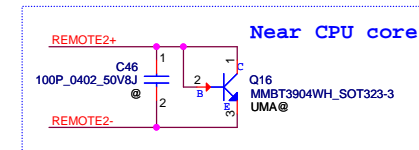
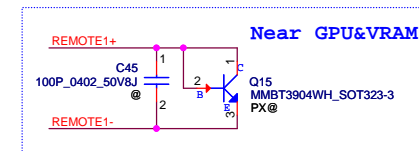
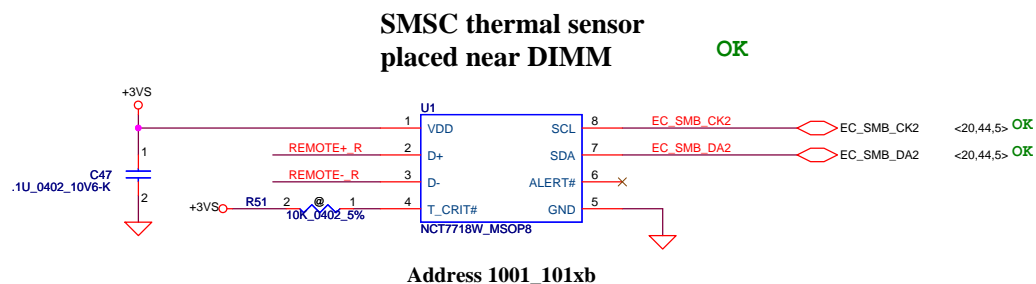
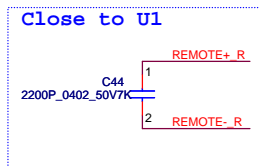


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				Date:	Thursday, February 20, 2014	Sheet 37 of 60

DL1/DL2
1'S PN:SC300003M00

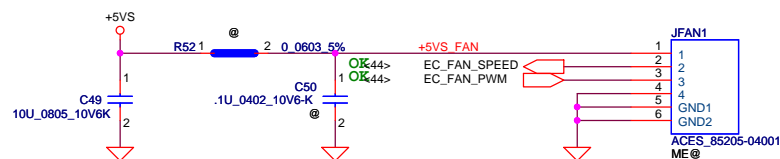


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				Date:	Thursday, February 20, 2014	Sheet 38 of 60



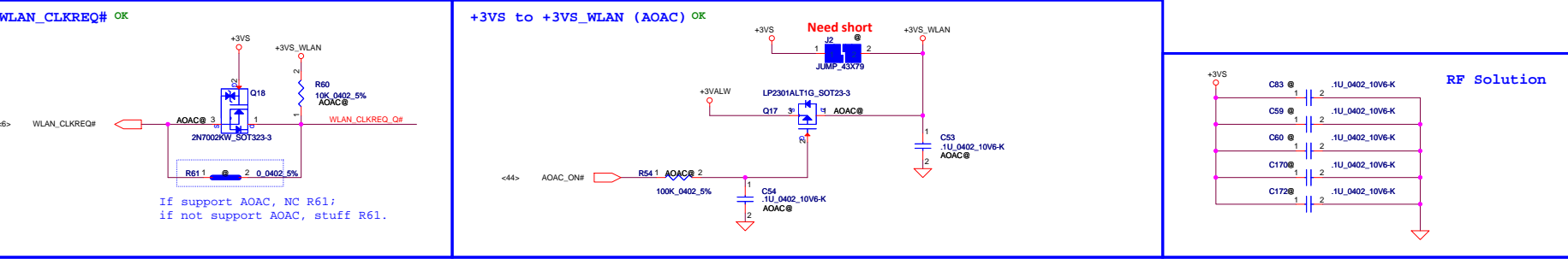
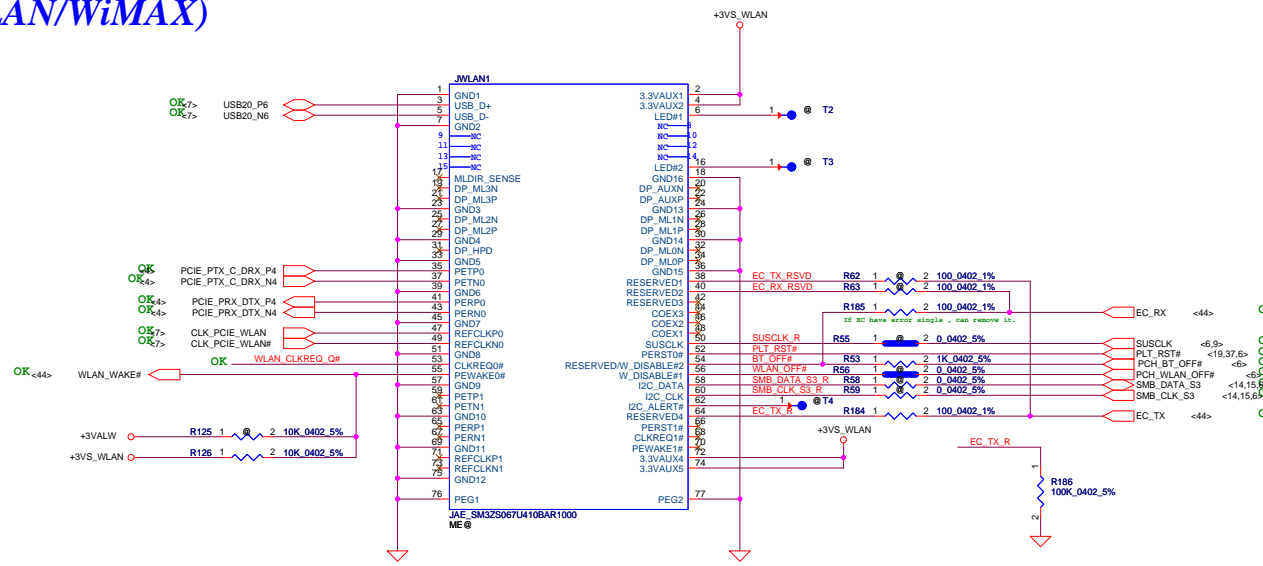
REMOTE+/_R, REMOTE1+/_R, REMOTE2+/_R:
Trace width/space:10/10 mil
Trace length:<8"

FAN Conn

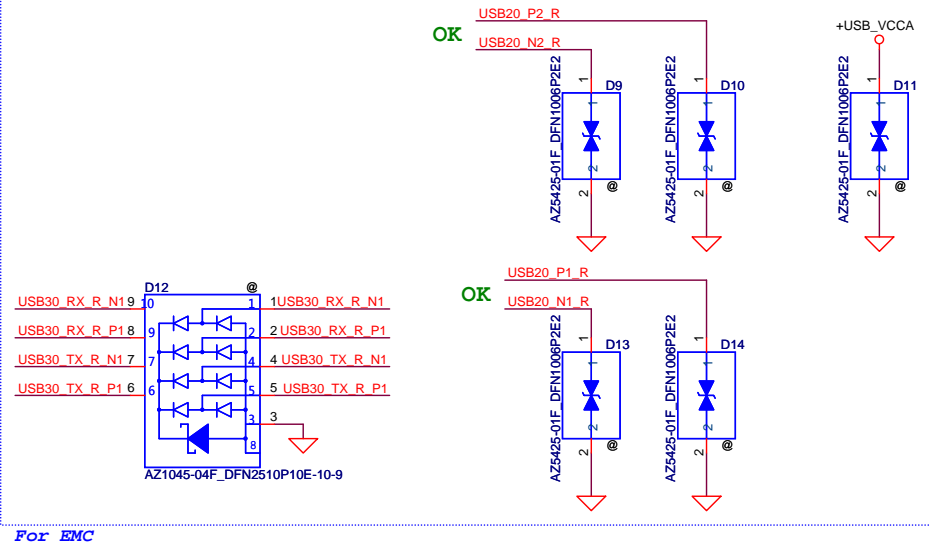
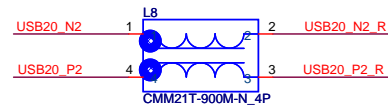
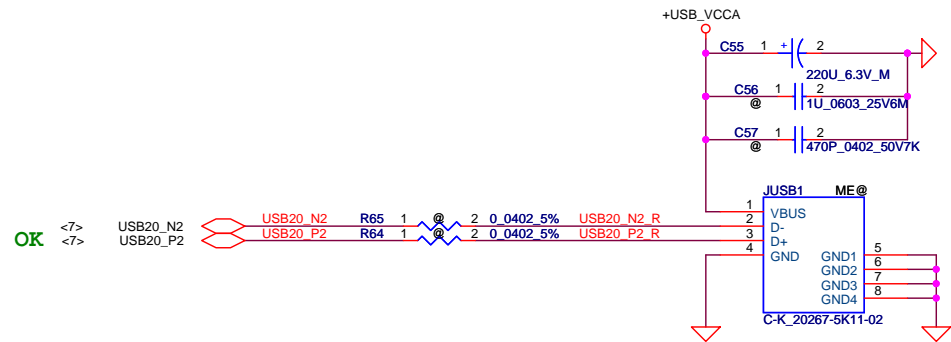
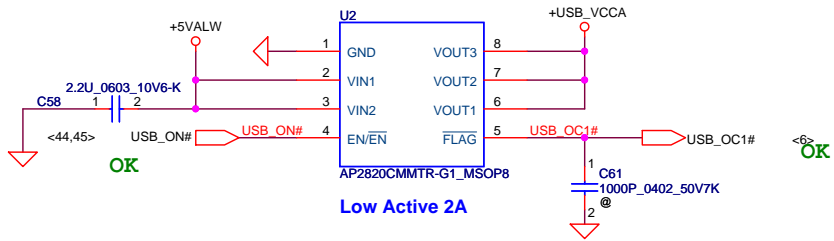


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Thermal sensor/FAN CONN	
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				Custom	NM-A281
				Date:	Thursday, February 20, 2014
				Sheet	39 of 60

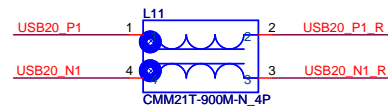
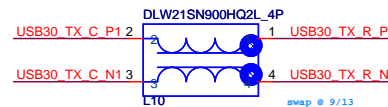
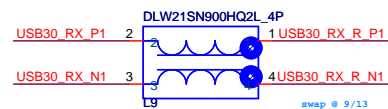
Mini-Express Card(WLAN/WiMAX)



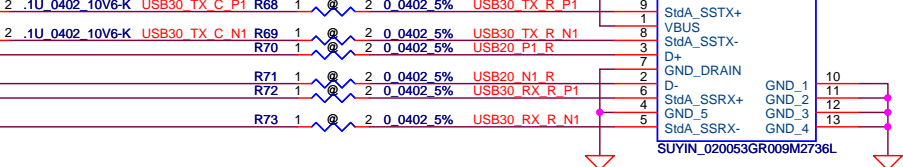
LEFT SIDE USB3.0 PORT X2



For EMC

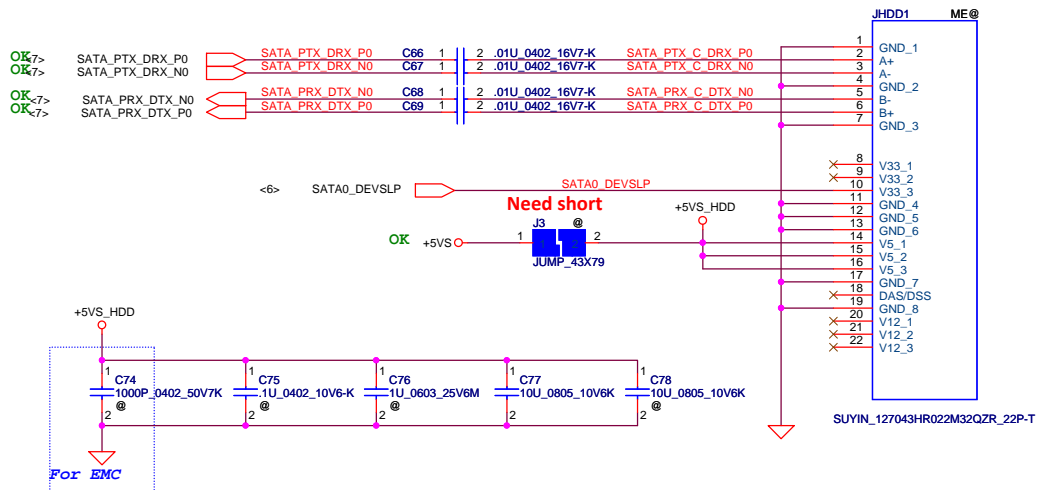


For EMC

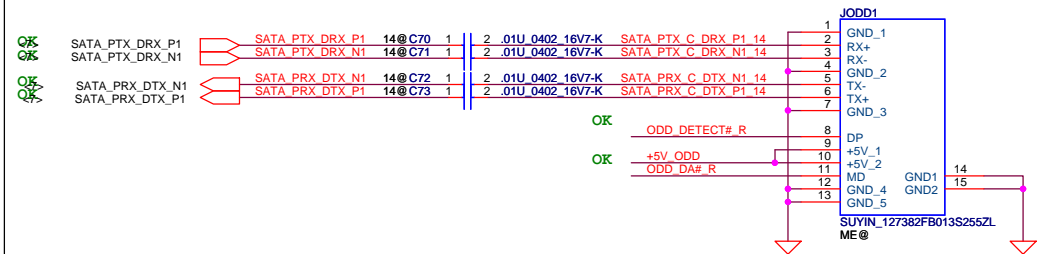


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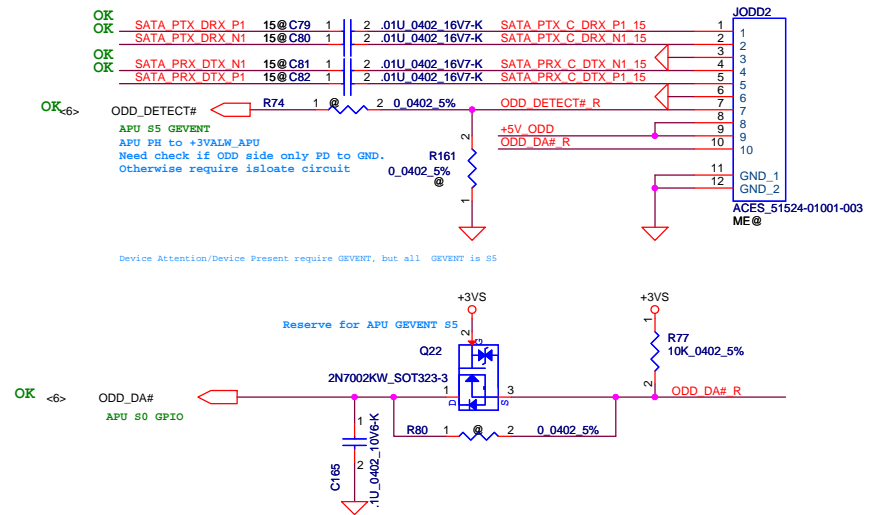
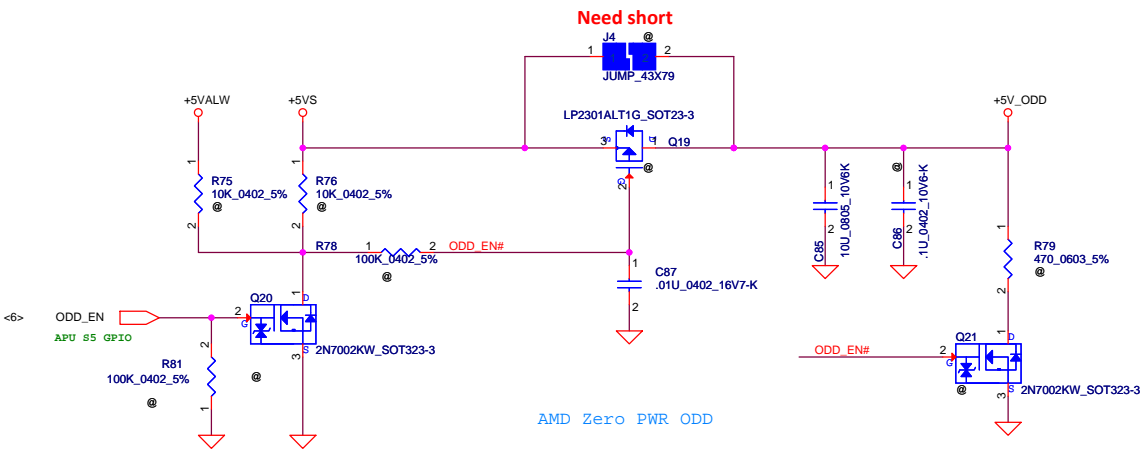
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USB2.0/USB3.0 PORT (LEFT)			
Size Custom	Document Number	Rev	
	NM-A281	0.4	

SATA HDD Conn.


FOR 14"
SATA ODD Conn.

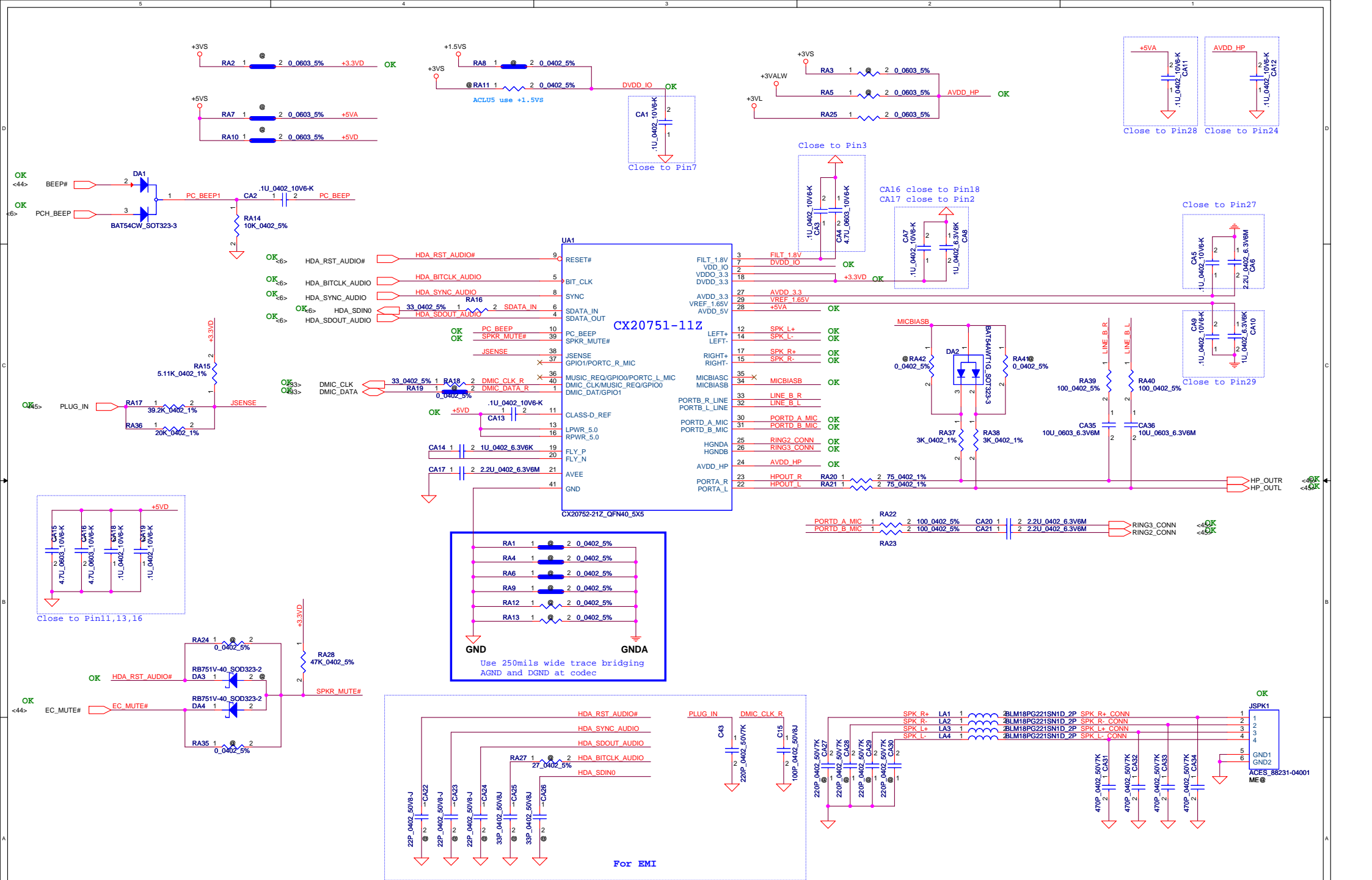


FOR 15"
SATA ODD FFC Conn



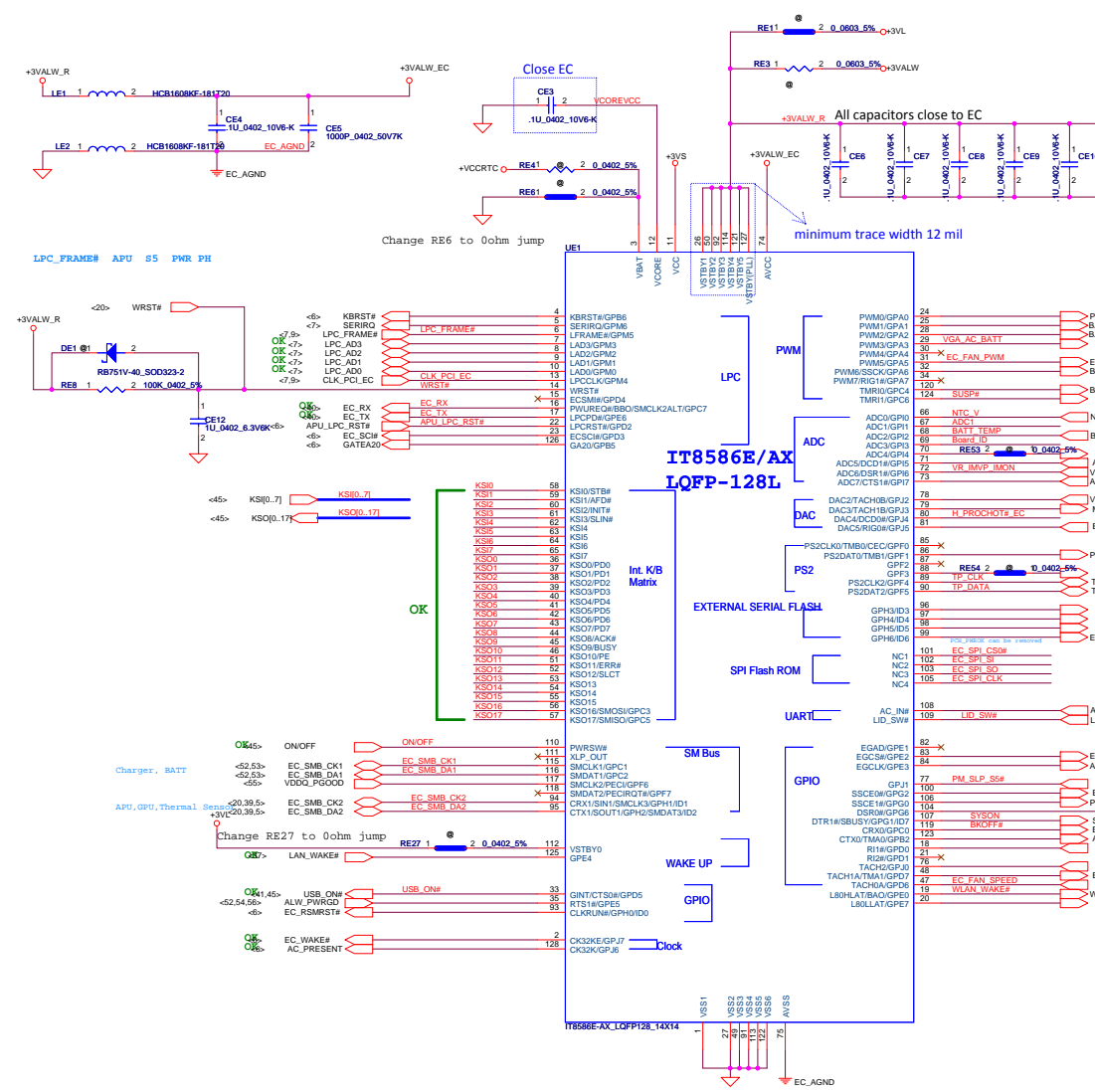
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Issued Date	2013/08/08	Deciphered Date	2013/08/05
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Title			
HDD/ODD CONN			
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Custom	NM-A281	0.4	
Date:	Thursday, February 20, 2014	Sheet	42 of 60



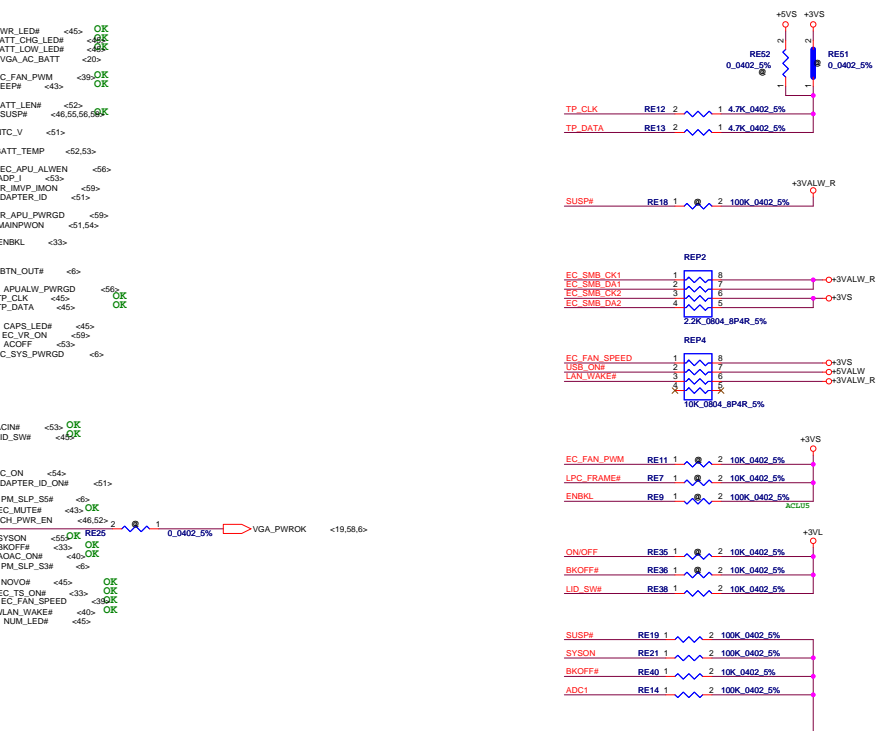
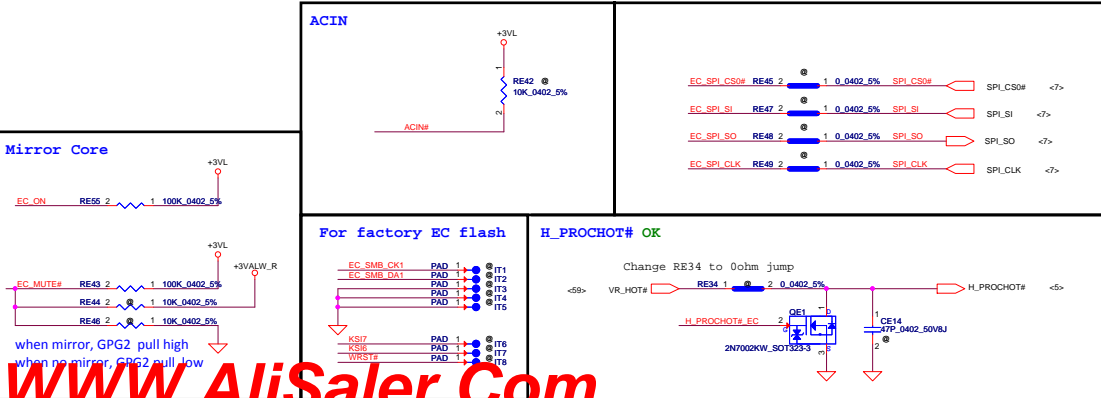
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Issued Date	2013/08/08	Deciphered Date	2013/08/05
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Codec_CX20752		Document Number	Custom
Date: Thursday, February 20, 2014		Sheet	43 of 60
Rev		NM-A281	
		0.4	



BORAD ID Config

Vcc	RE33	RE34	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Phase
3.3V +/- 5%	100K +/- 1%					
Board ID	RE34					
0	0K +/- 5%	0 V	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V		
2	18K +/- 5%	0.436 V	0.503 V	0.538 V		
3	33K +/- 5%	0.712 V	0.819 V	0.875 V		
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V		
5	24K +/- 5%	0.612 V	0.638 V	0.664 V		



EMI/ESD Req

Component	Value	Location
CLK_PCL_EC	RE2	1 100K 0402_5%
APU_LPC_RST#	RE3	1 100K 0402_5%
SYSON	RE4	1 100K 0402_5%
BATT_TEMP	CE16	1 100P 0402_50VJ
ACIN#	CE17	1 100P 0402_50VJ
ON/OFF	CE18	1 1U 0402_6.3V8K
WLAN_WAKE#	CE19	1 1U 0402_10V6-K

Security Classification

Classification	LC Future Center Secret Data
Issued Date	2013/08/08
Deciphered Date	2013/08/05

Title

EC ITE8586LQFP

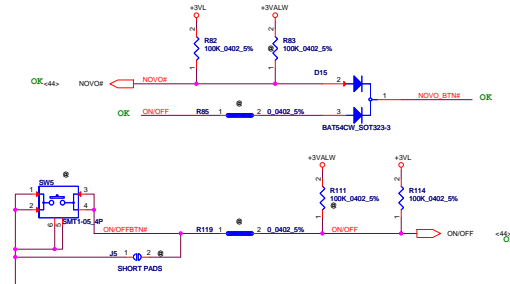
Document Number

NW-A281

Date

Thursday, February 20, 2014 1:58:44 PM

ON/OFF switch

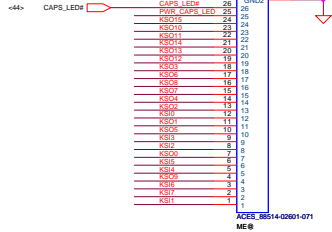


TP/B Connector

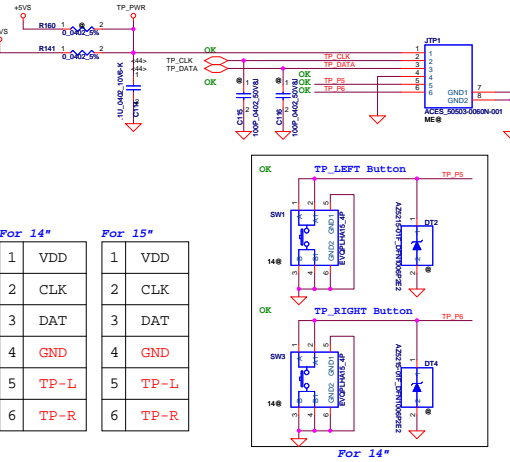
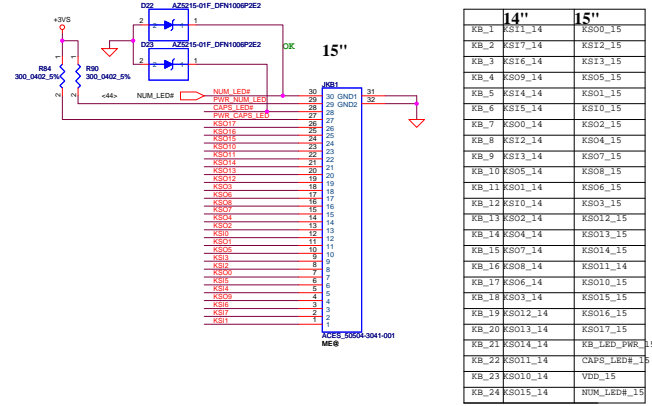
K/B Connector



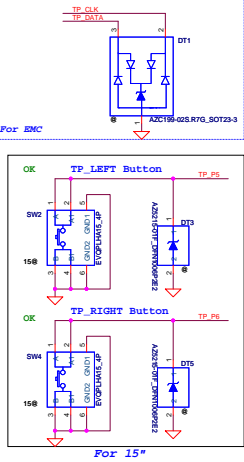
14"



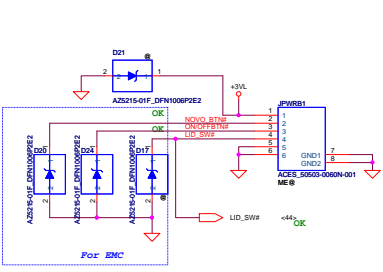
15"



For 14"	For 15"
1 VDD	1 VDD
2 CLK	2 CLK
3 DAT	3 DAT
4 GND	4 GND
5 TP-L	5 TP-L
6 TP-R	6 TP-R

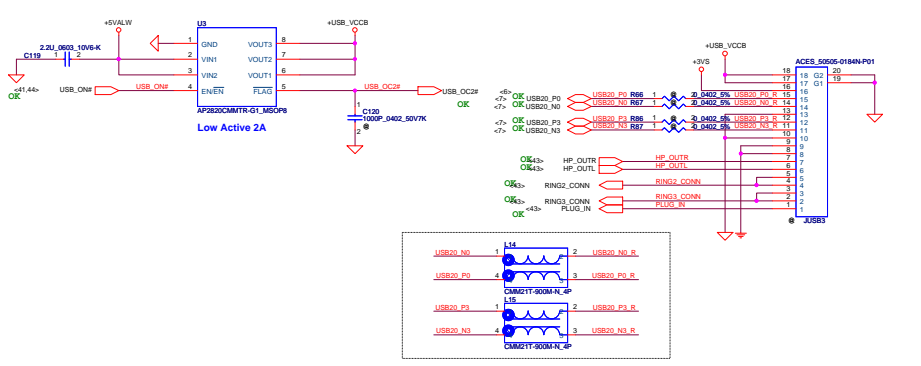


PWR/B Connector

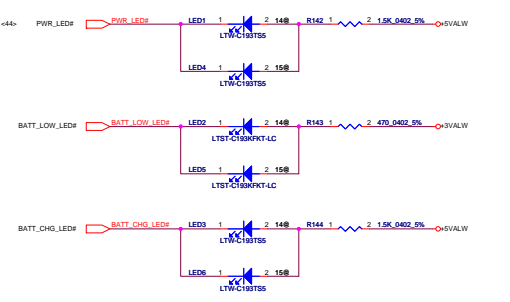


USB I/O Connector

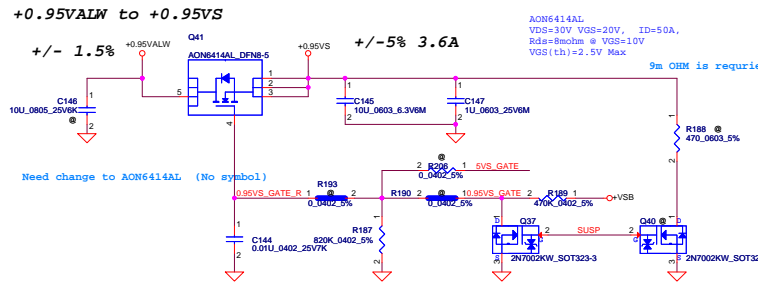
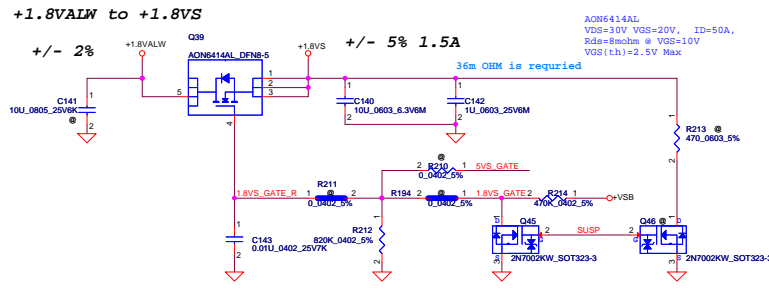
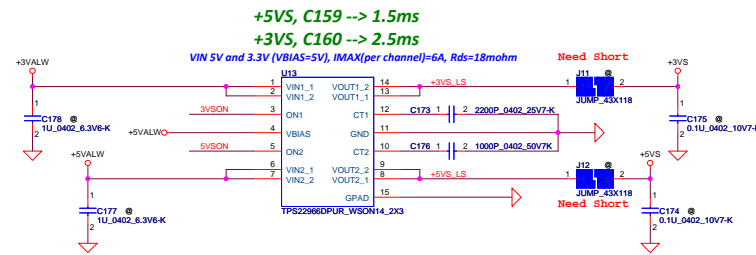
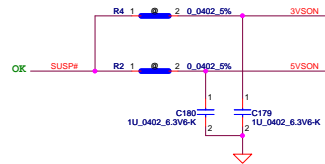
Right Side USB2.0 Port X 1 (USB/B)

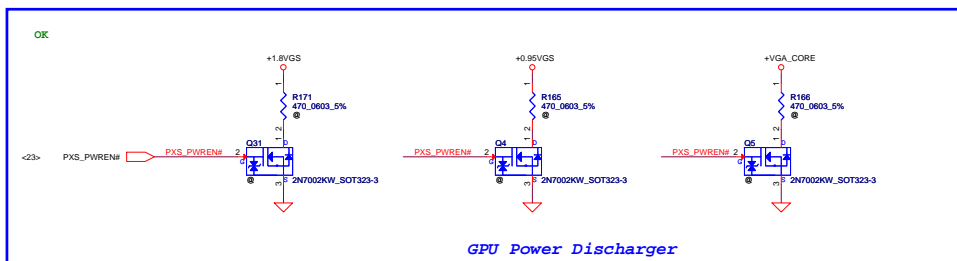
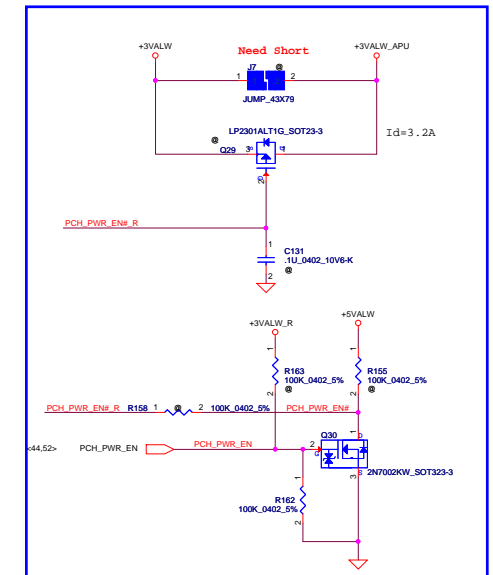
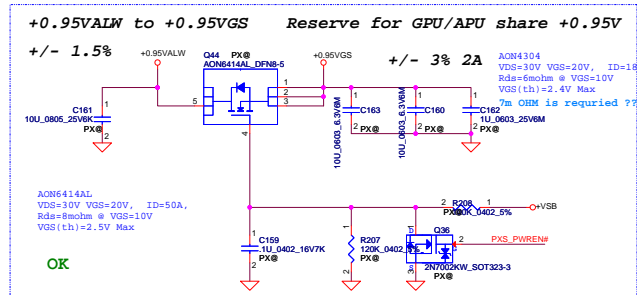
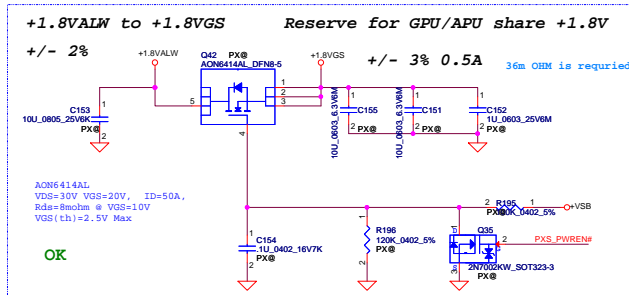



LED



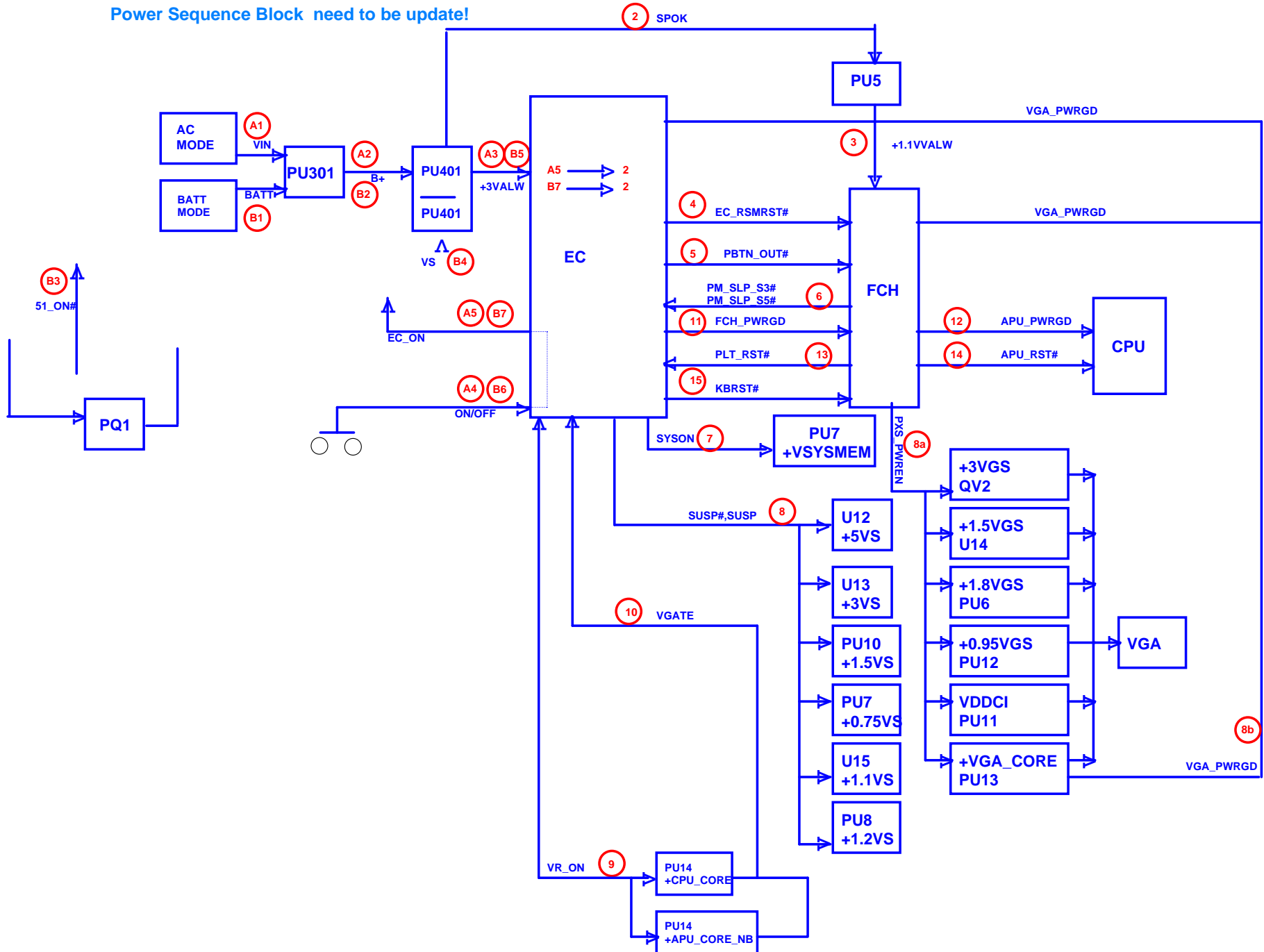
+5VALW To +5VS OK
+3VALW To +3VS





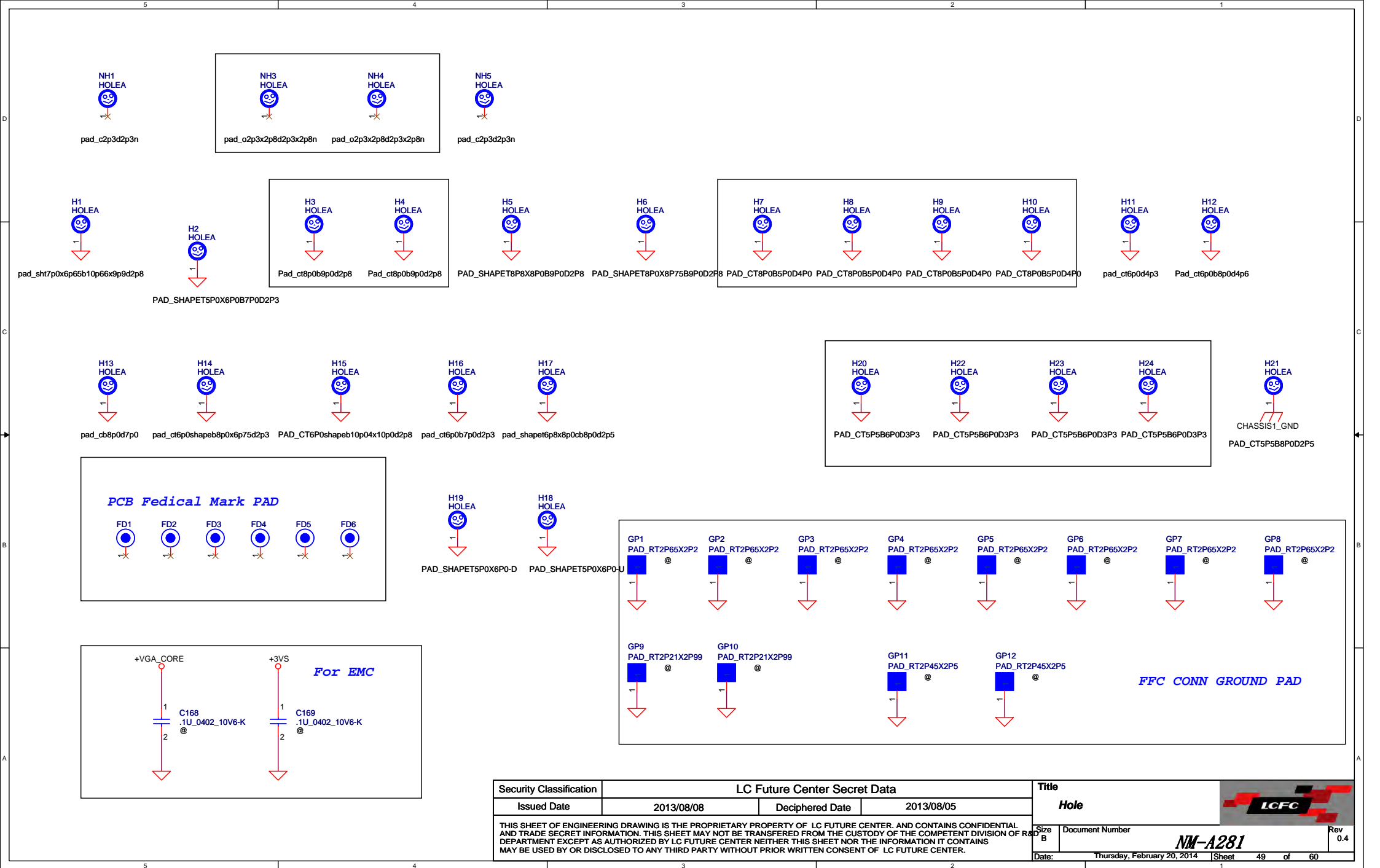
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Issued Date	2013/06/15	Deciphered Date	2013/08/15	DC V TO VS INTERFACE		
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				Date	NW-4281	0.4
				Thursday, February 20, 2014 12:00 PM 46 of 60		

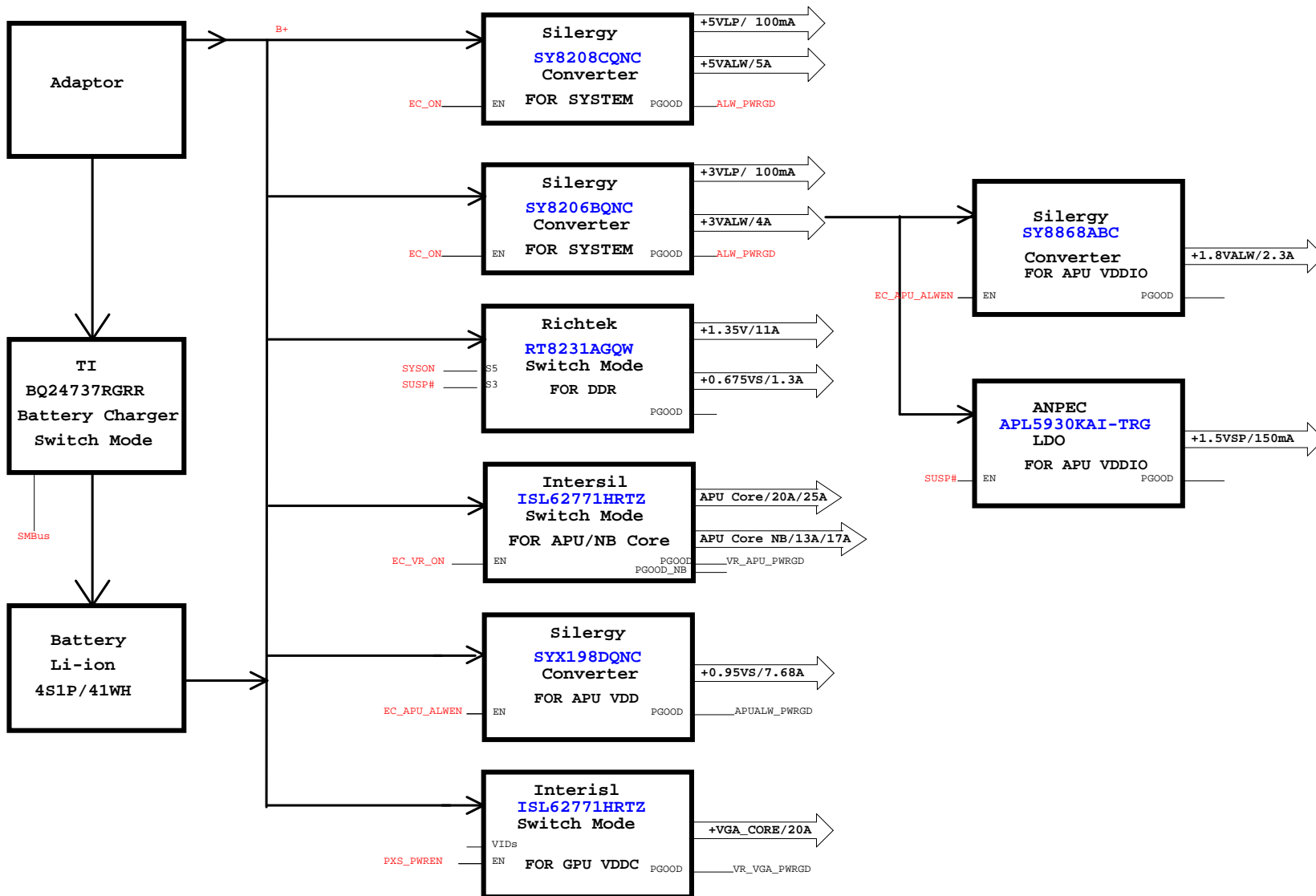
Power Sequence Block need to be update!




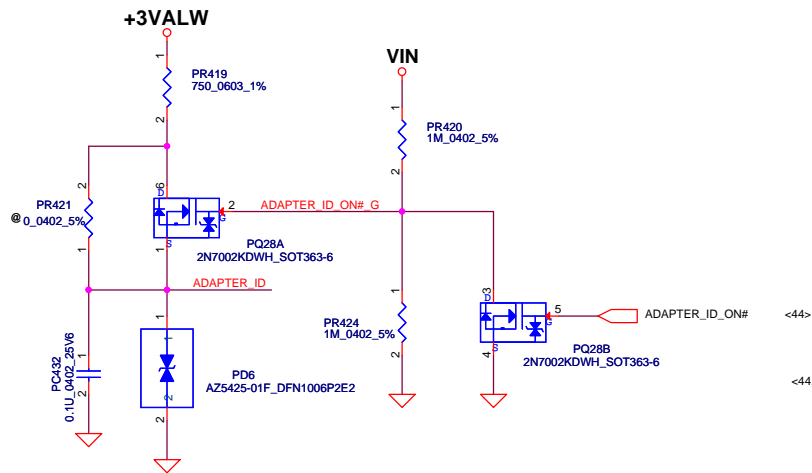
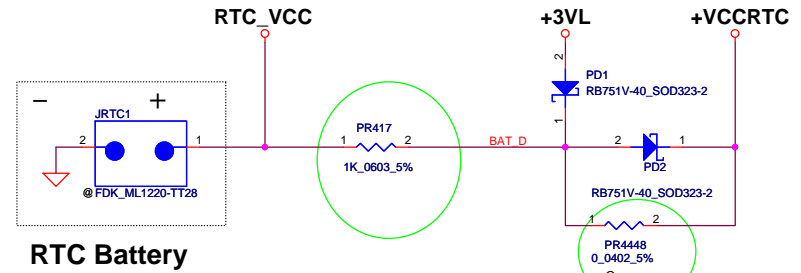
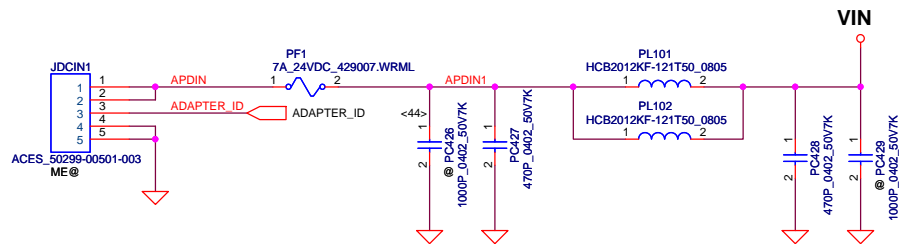
LC Future Center Secret Data			
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Title		Rev	
Power sequence Block		0.4	
Size	Document Number	NM-A281	
Custom			
Date:	Thursday, February 20, 2014	Sheet	47 of 60

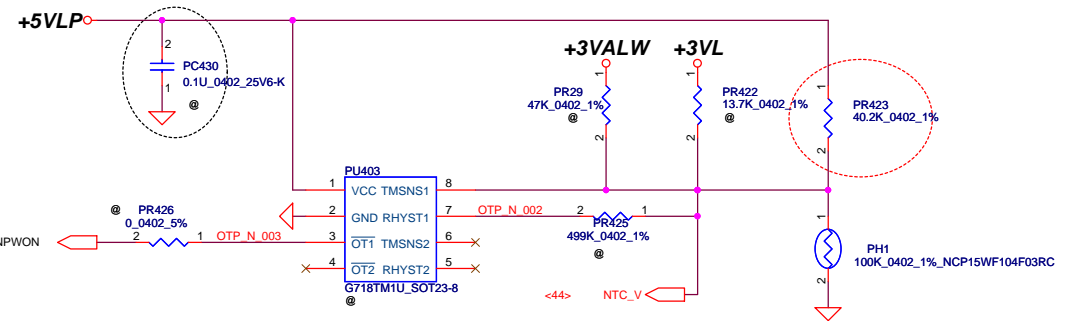




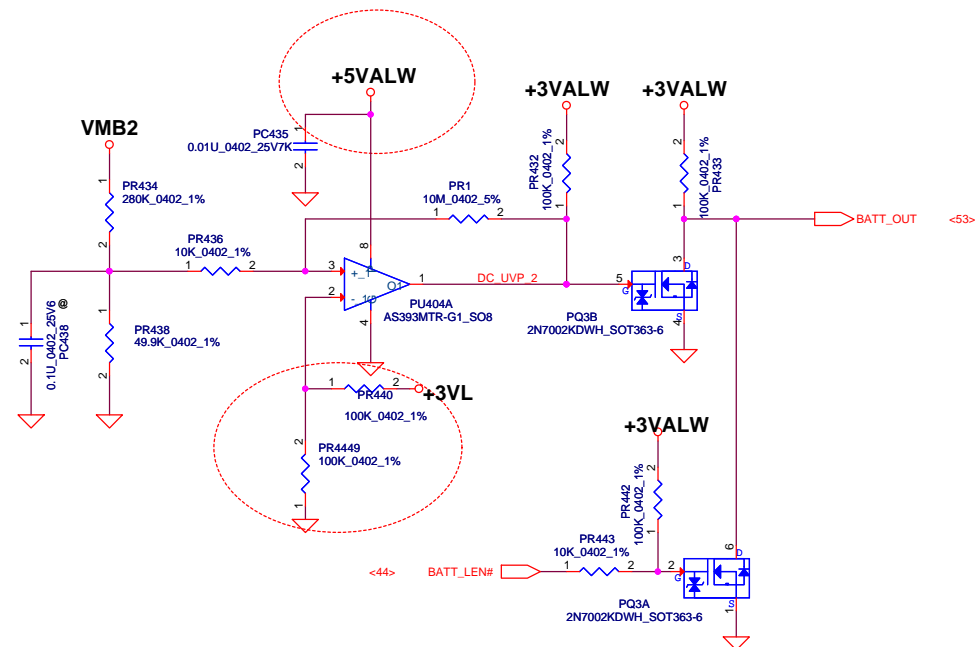
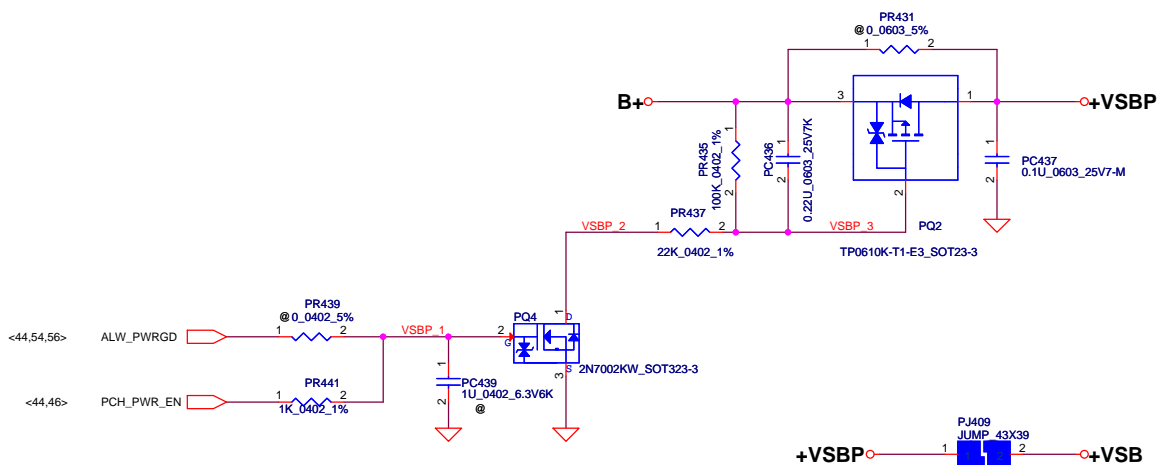
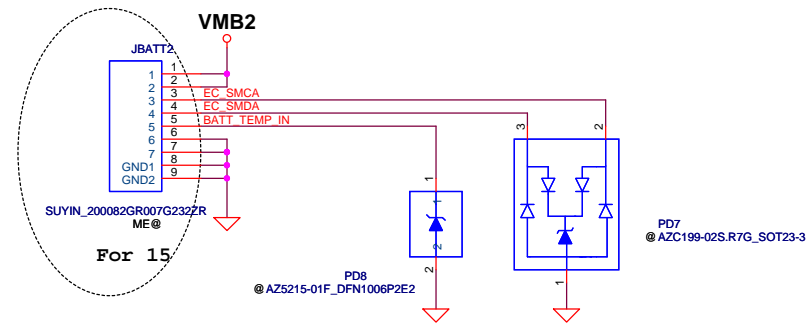
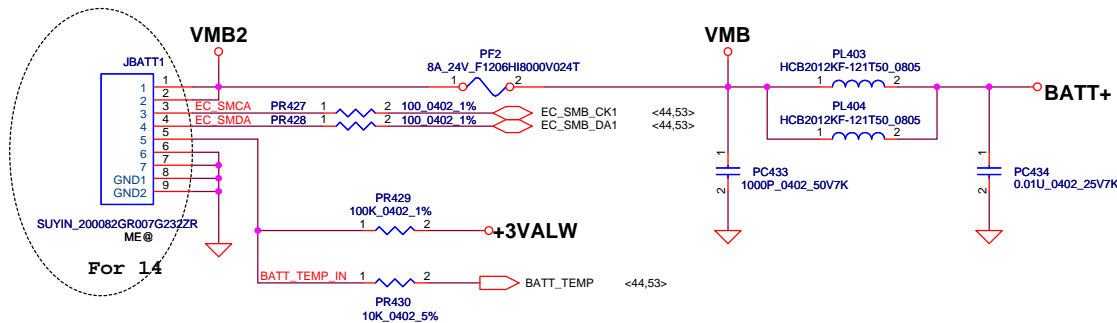
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Issued Date	2013/08/15	Deciphered Date	2013/08/15	Size			
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				Date	Thursday, February 20, 2014		Sheet 50 of 80

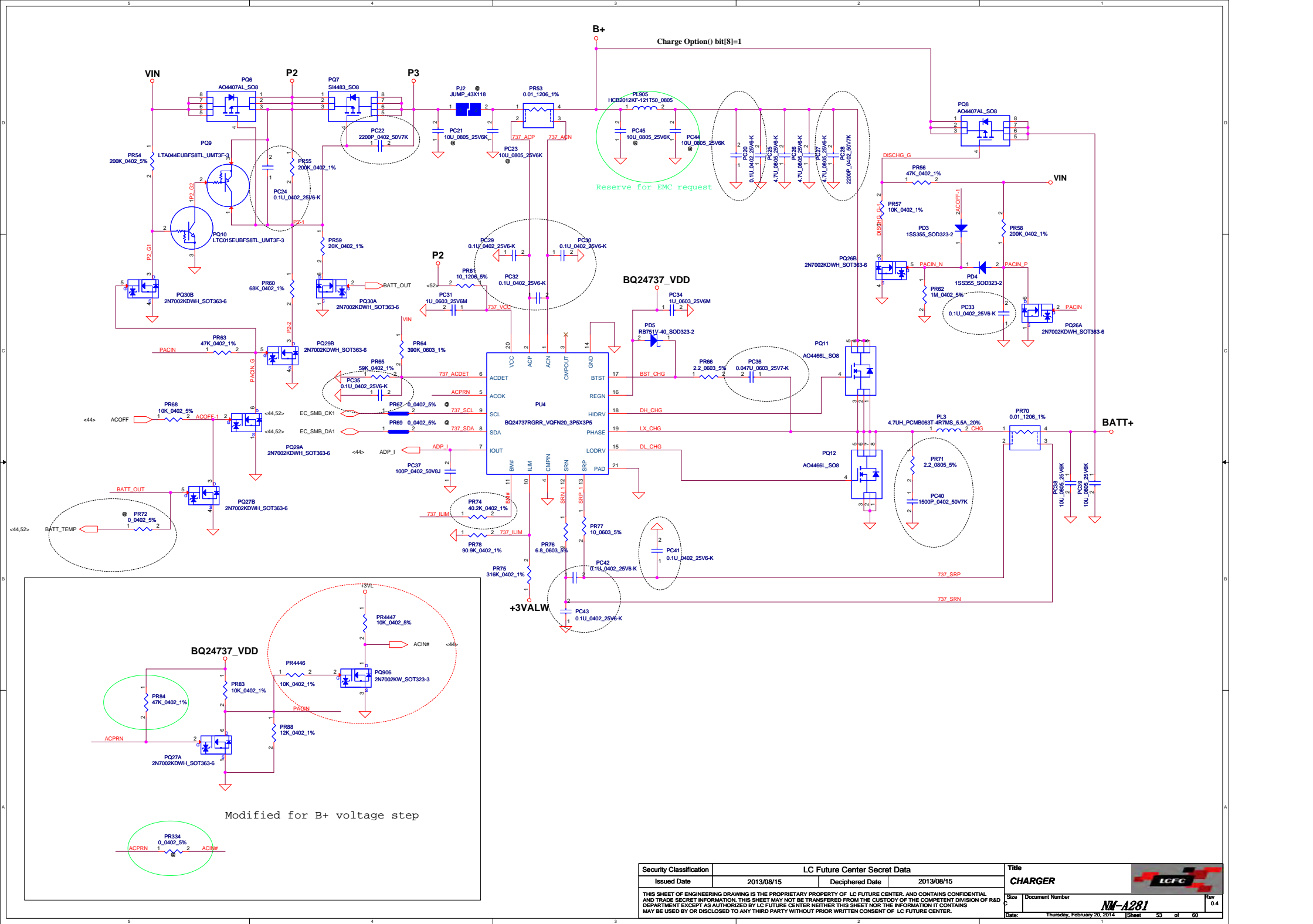


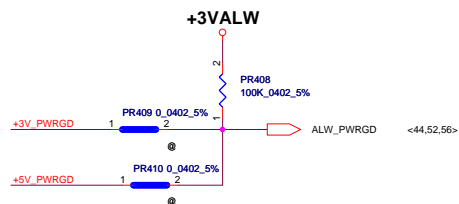
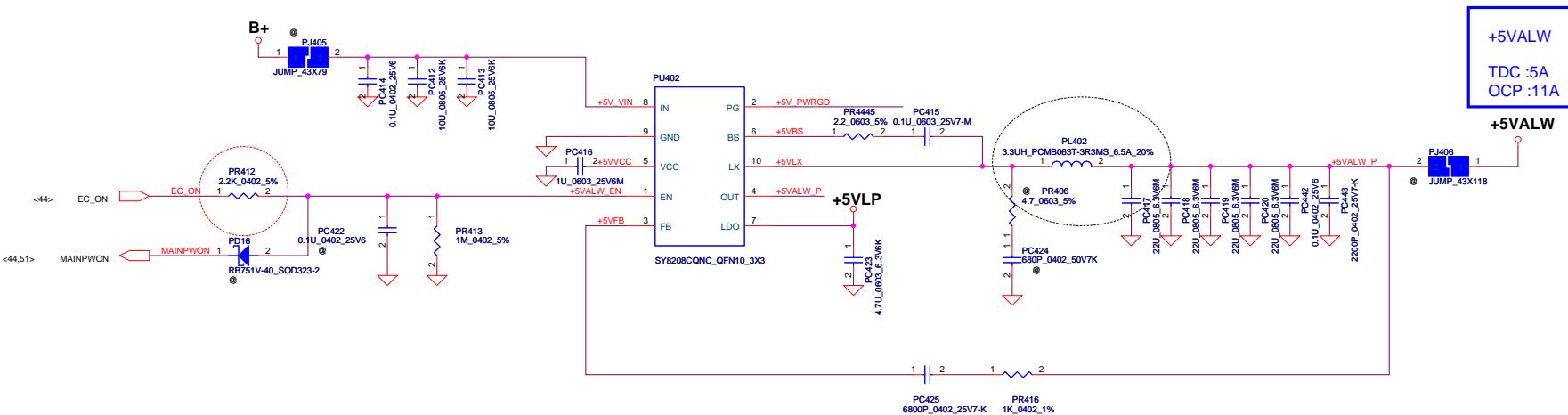
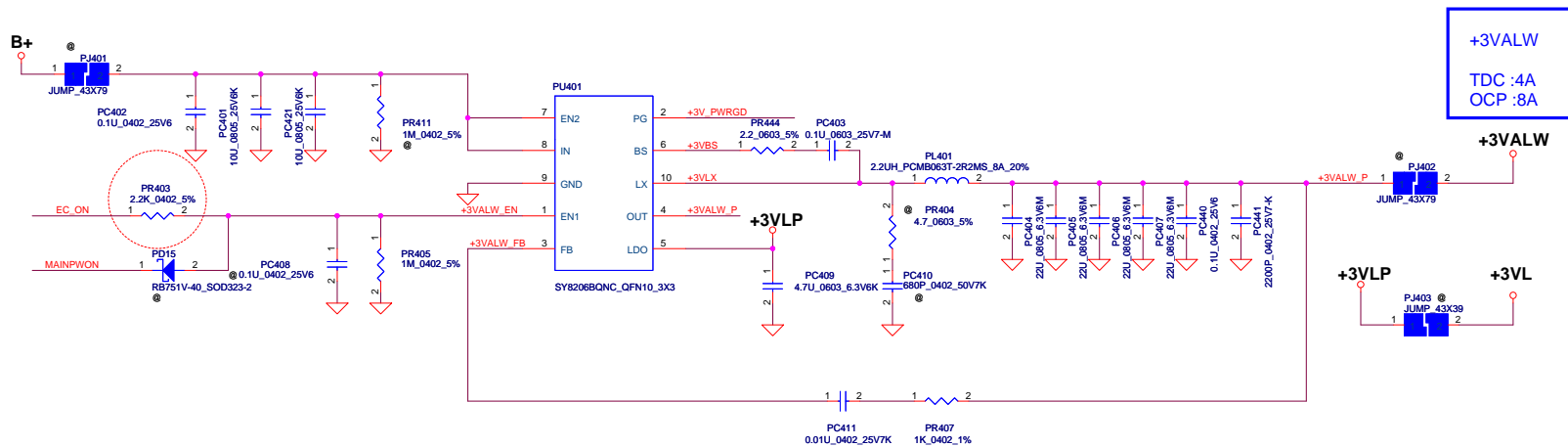
PH1 under CPU bottom side :
CPU thermal protection at 92+/-3 degree C
Recovery at 56 +/-3 degree C

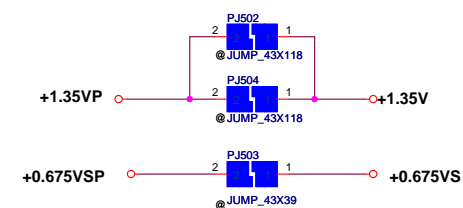


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				Date:	Thursday, February 20, 2014	Sheet 51 of 60

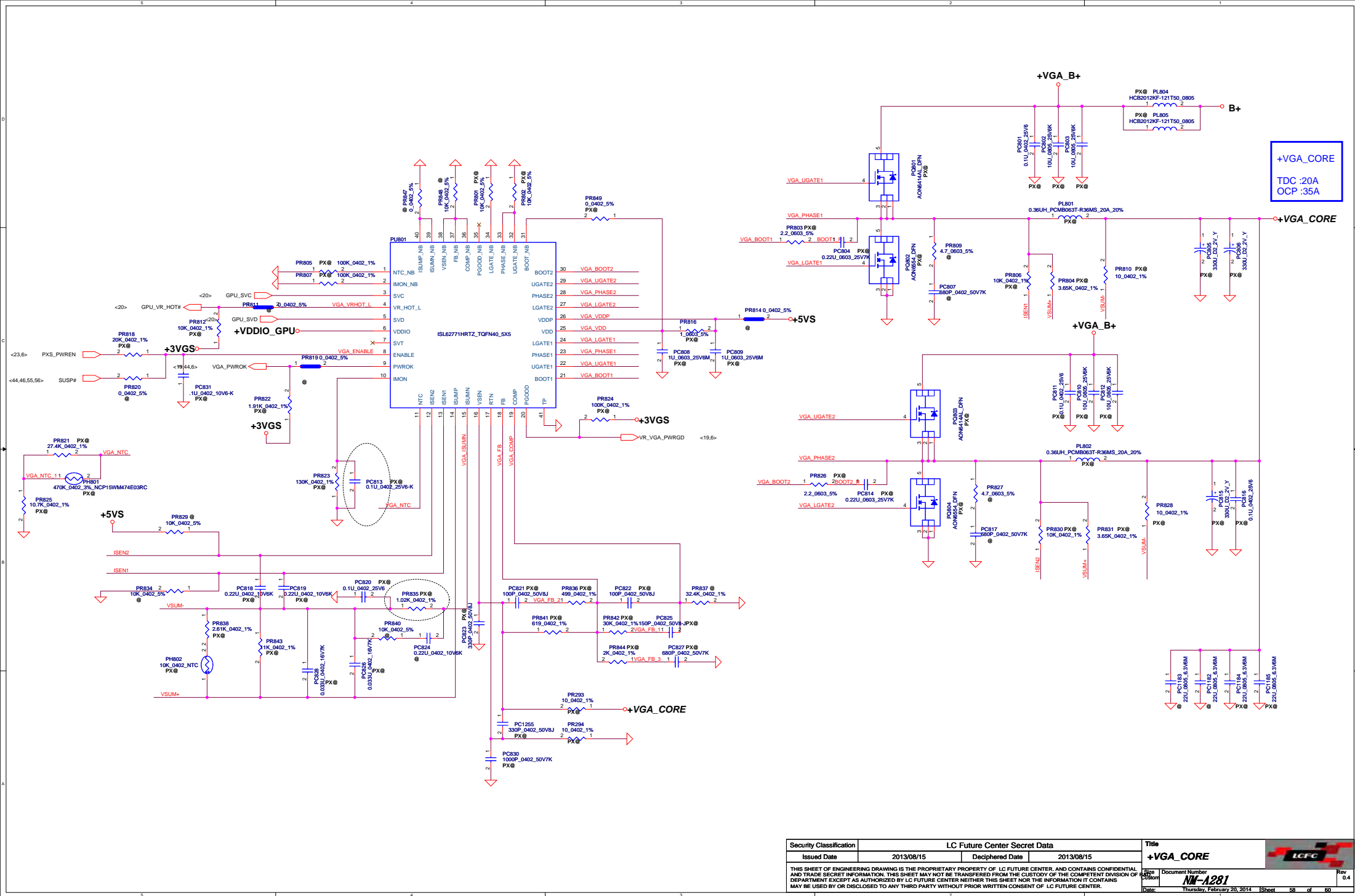


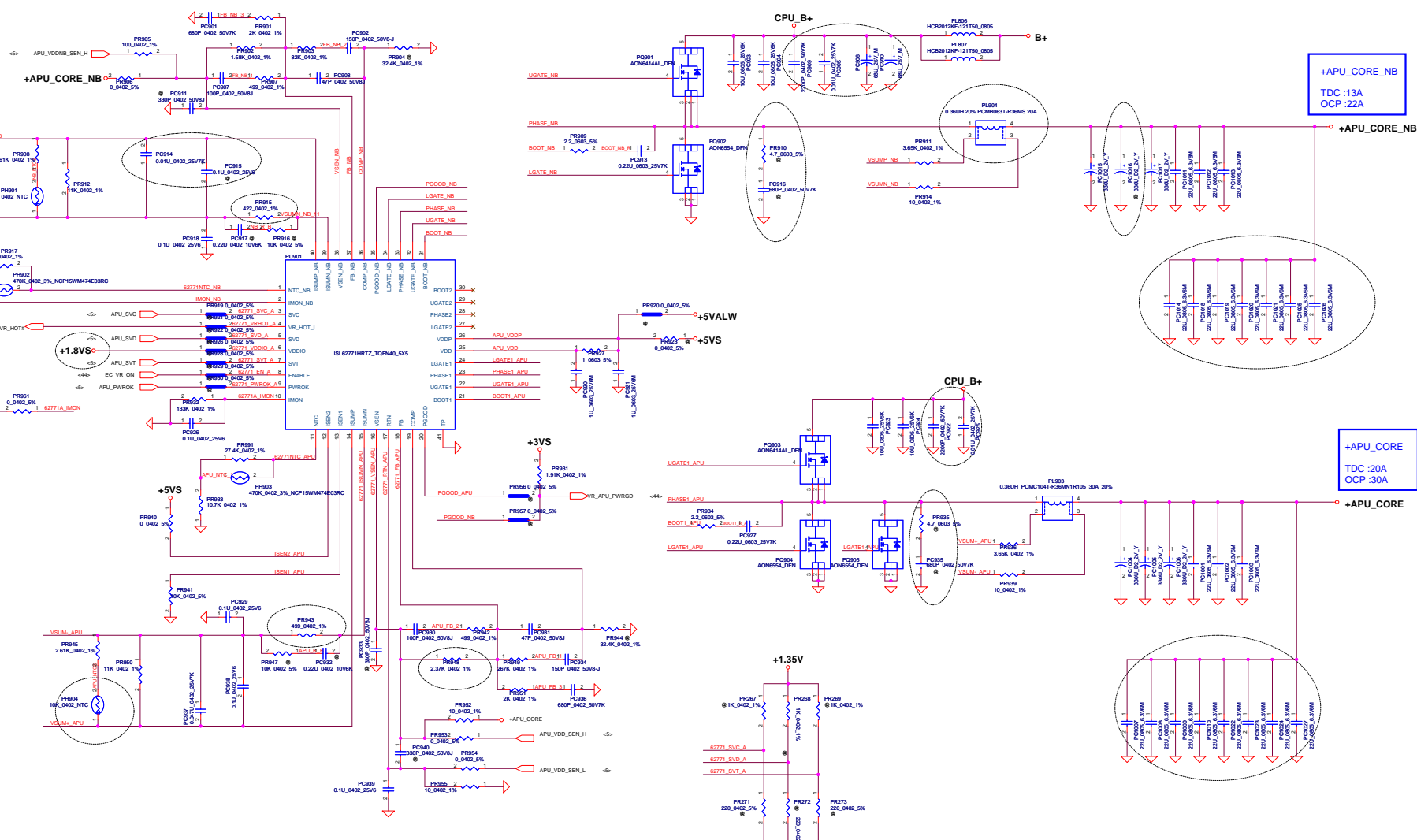






5		4		3		2		1		
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C								C		
B								B		
A								A		
Security Classification						LC Future Center Secret Data		Title		
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						Date: Thursday, February 20, 2014				Sheet 57 of 60
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SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V(Default)

